

4-channel analog input class-D automotive audio amplifier with Hi-Fi audio quality, advanced diagnostics and 2 MHz switching frequency



LQFP48L exposed pad up (7x7x1.4 mm)

Product summary			
Order code	Package	Packing	
HFA80A-F2Y	LQFP48L 7x7x1.4 mm	Tray	
HFA80A-F2T		Tape and reel	

Features



- AEC-Q100 qualified
- Supply operating range: 4.5 V 18 V
- EMI compliant to CISPR25 level V
- Class-D BTL outputs
- Battery load dump compatible (40 V)
- Reduced size and cost of output LC thanks to 2 MHz switching PWM
- Extended audio band support
- Multiple load configurations:
 - Able to drive 4 Ω and 2 Ω speaker loads
 - Both speaker and line driver options
- MOSFET power outputs allowing high output power capability:
 - Typ 4 x 28.5 W/4 Ω at 14.4 V, 1 kHz, THD = 10%
 - Typ 4 x 23 W/4 Ω at 14.4 V, 1 kHz, THD = 1%
 - Typ 4 x 49 W/2 Ω at 14.4 V, 1 kHz, THD = 10%
 - Typ 4 x 39 W/2 Ω at 14.4 V, 1 kHz, THD = 1%
- Audio performances at 4 Ω, 14.4 V, 1 kHz:
 - THD 0.015% typ at 1 W, 1 kHz on 4 Ω loads
 - Output noise 52 typ μV at 26 dB gain
 - Crosstalk 86 dB typ at 1 W, 1 kHz on 4 Ω loads
 - PSRR 80 dB typ at 1 W, 1 kHz on 4 Ω loads
- Fast turn-on and very low latency for high-speed audio processing applications
- I²C full configurability with channel independent mute/play/gain selection/ diagnostic
- 4 I²C addresses
- I²C bus driving: fast I²C (1Mhz clock) option
- Output PWM clock spread spectrum
- Full diagnostic matrix with info available both on I²C and CD/DIAG pin:
 - Independent by-channel DC and AC load detection diagnostic with selectable threshold
 - Startup diagnostic for shorts to VCC/GND
 - Overcurrent protection with configurable threshold (2 selectable)
 - Input voltage DC offset detector
 - Free-running output current offset detector
- Thermal protection and thermal warning (4 thermal warnings)
- DAM (digital admittance meter)
- Synchronization input/output pin
- Immune to pop/tick noise at turn on/off, battery variations, during diagnostic
- Legacy (backup mode without I²C control)
- ESD integrated protections (2 kV HBM, 500 V/750 V corner CDM)
- LQFP48L exposed pad up package



Description

The HFA80A is a new STMicroelectronics class-D audio amplifier, specifically designed for automotive applications in BCD9s technology.

The HFA80A integrates advanced solutions for an excellent radiated noise immunity combined with the advantages of 2 MHz switching PWM class-D output stages. This configuration allows outstanding audio performances while designing a compact and inexpensive application.

The HFA80A supports wide band applications with extremely low level of noise and low THD. Moreover, it features a broad diagnostics matrix able to support the most demanding OEM requirements in terms of speaker control and system robustness/reliability. The HFA80A supports start/stop cranking down to 4.5 V and is housed in a very compact and thin LQFP 7x7 package, making it suitable for any level of automotive application.

DB5280 - Rev 1 page 2/16



1 Block diagram and pin description

1.1 Block diagram

DrvBias **PVCCx** SGndx OUT1+ Channel 1 OUT1-Powerstage IN1+ IN1-OUT2+ Channel 2 IN2+ Powerstage OUT2-**PWM** Gate IN2modulators Drives Channel 3 OUT3+ IN3+ Differential Analog input IN3-Powerstage ► OUT3-IN4+ IN4-Channel 4 OUT4+ Powerstage OUT4-VBAT | ► PGNDx Reference and Protection Enable C control logic Ext3V3 Diagnostics Regulator 1.8V & -CD/Diag Dvdd(D1V8) Digital Core PLL & OSC SYNCIN/OUT SCL 10 SDA I2C Control ADDSel C SUBx **HWMute**

Figure 1. Block diagram

DB5280 - Rev 1 page 3/16

13 14 15 16 17 18 19 20 21 22 23 24

DRVBIAS SUB1

SYNCIN/OUT

DVDD(D1V8)



Pin description 1.2

24 23 22 21 20 19 18 17 16 15 14 13

DRVBIAS

SGND SGND IN/OUT COLV8)

SYNCIN/OUT [DVDD(D1V8) [

ADDSEL

PGND1 | 12 OUT1+ | 12 OUT1+ | 12 OUT1+ | 12 VBAT | 12 NC | 12 SUB1 | 12

ENABLE | OUT4-| OUT4+ | PVCC4 OUT4+ PVCC3 36 PVCC3 □ IN4-36 IN4-OUT3-35 IN4+ OUT3-35 IN4+ 2 PGND3 34 SGND SGND [PGND3 О з 34 PGND3 [33 IN3-PGND3 IN3-33 OUT3+ 32 □ IN3+ IN3+ 32 OUT3+ PVCC3 31 SVR SVR [31 PVCC3 PVCC2 30 EXT3V3 EXT3V3 30 PVCC2 OUT2+ 29 IN2+ IN2+ 29 OUT2+ PGND2 [28 ☐ IN2-IN2-28 PGND2 9 SGND [PGND2 [SGND 27 PGND2 27 10 10 OUT2-IN1+ OUT2-26 IN1+ 26 11 PVCC2 | IN1-PVCC2 IN1-25 12

Figure 2. Device pinout

Table 1. Pin function

#	Name	Function	Definition	Internal structure
1	IN4-	CH 4, half bridge minus	Input	-
2	IN4+	CH 4, half bridge plus	Input	-
3	SGND	Signal ground	Supply	-
4	IN3-	CH 3, half bridge minus	Input	-
5	IN3+	CH 3, half bridge plus	Input	-
6	SVR	Supply voltage rejection	Internal reference	-
7	EXT3V3	Auxiliary external 3.3 V supply	Supply	-
8	IN2+	CH 2, half bridge plus	Input	-
9	IN2-	CH 2, half bridge minus	Input	-
10	SGND	Signal ground	Supply	-
11	IN1+	CH 1, half bridge plus	Input	-
12	IN1-	CH 1, half bridge minus	Input	-
13	ADDSEL	Address selection	Input	-
14	DVDD(D1V8)	Digital power supply	Supply	-
15	SYNCIN/OUT	Synchronization clock in/out	Input/Output	Push-pull
16	SGND	Signal ground	Supply	-
17	DRVBIAS	Gate driver Bias	Internal reference	-
18	SUB1	Ground die substrate pin	Supply	-
19	NC	Not connected	-	-
20	VBAT	Battery voltage pin	Supply	-
21	PVCC1	CH 1, power supply	Supply	-

DB5280 - Rev 1 page 4/16



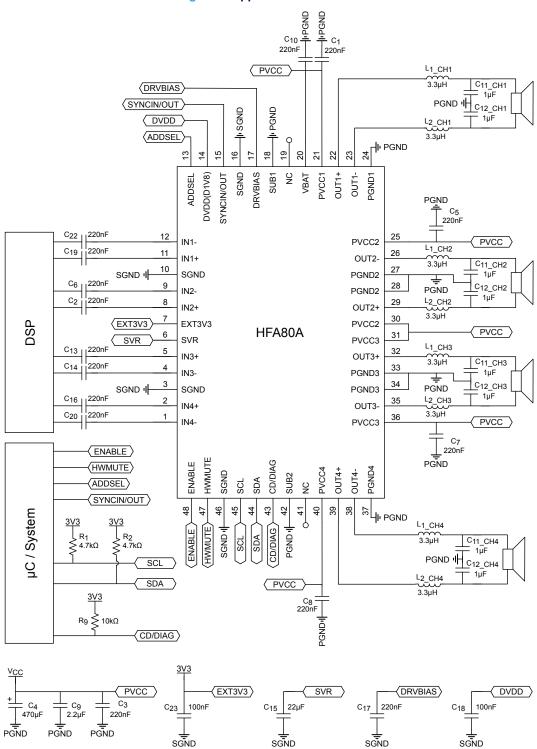
#	Name	Function	Definition	Internal structure
22	OUT1+	CH 1, half bridge plus	Output	-
23	OUT1-	CH 1, half bridge minus	Output	-
24	PGND1	CH 1, power ground	Supply	-
25	PVCC2	CH 2, power supply	Supply	-
26	OUT2-	CH 2, half bridge minus	Output	-
27	PGND2	CH 2, power ground	Supply	-
28	PGND2	CH 2, power ground	Supply	-
29	OUT2+	CH 2, half bridge plus	Output	-
30	PVCC2	CH 2, power supply	Supply	-
31	PVCC3	CH 3, power supply	Supply	-
32	OUT3+	CH 3, half bridge plus	Output	-
33	PGND3	CH 3, power ground	Supply	-
34	PGND3	CH 3, power ground	Supply	-
35	OUT3-	CH 3, half bridge minus	Output	-
36	PVCC3	CH 3, power supply	Supply	-
37	PGND4	CH 4, power ground	Supply	-
38	OUT4-	CH 4, half bridge minus	Output	-
39	OUT4+	CH 4, half bridge plus	Output	-
40	PVCC4	CH 4, power supply	Supply	-
41	NC	Not connected	-	-
42	SUB2	Ground die substrate pin	Supply	-
43	CD/DIAG	Clipping detector and diagnostic	Output	Open-drain
44	SDA	I ² C data	Input/Output	Open-drain
45	SCL	I ² C clock	Input	-
46	SGND	Signal ground	Supply	-
47	HWMUTE	Hardware mute	Input	Internal pull-up
48	ENABLE	Enable	Input	-

DB5280 - Rev 1 page 5/16



Application schematic

Figure 3. Application schematic



DB5280 - Rev 1 page 6/16



3 Electrical specifications

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{CC max}	DC supply pins [VBAT, PVCC(x)]	-0.3 to 40	V
OUT _(x) +, OUT _(x) -	Output ± pin	-0.3 to 25	V
EXT3V3	Voltage on EXT3V3 pin	-0.3 to 4.6	V
IN _(x) +, IN _(x) -	Analog input ± max	-0.3 to 4.6	V
I2C _{data} , I2C _{clk}	I ² C bus pins [SDA, SCL]	-0.3 to 4.6	V
SYNCHIN/OUT	Synchronization pin	-0.3 to 4.6	V
ADDSEL	Address selection pin	-0.3 to 4.6	V
ENABLE	Enable pin	-0.3 to 4.6	V
CD/DIAG	Clipping detector and diagnostic pin	-0.3 to 4.6	V
HWMUTE	Hardware mute pin	-0.3 to 4.6	V
GND _{max}	Voltage difference between ground pins [SGND, $PGND_{(x)}$, $SUB_{(x)}$]	-0.3 to 0.3	V
DRVBIAS	Gate driver bias pin (1)	-0.3 to 20	V
SVR	Internal reference pin ⁽¹⁾	-0.3 to 4.6	V
DVDD(D1V8)	Digital power supply pin ⁽¹⁾	-0.3 to 2.5	V
T _{amb}	Ambient operating temperature	-40 to 125	°C
T _{stg} ,T _j	Storage and junction temperature	-55 to 150	°C
ESD _{HBM}	ESD protection HBM ⁽²⁾	2000	V
ESD	ESD protection CDM standard ⁽²⁾	500	V
ESD _{CDM}	ESD protection CDM corner ⁽²⁾	750	V

^{1.} Internal circuit output pin: not to be controlled externally.

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
Rthjc	Rth junction to case ⁽¹⁾	2.05	°C/W

By simulation with top cold plate as per Jedec best practice guidelines (JESD51) in contact with package top side (e-pad). Ambient temperature set to 85 °C.

DB5280 - Rev 1 page 7/16

^{2.} Conforming to ESD standard.



4 General description

The HFA80A is a quad channel, analog input, class-D BTL audio amplifier with advanced diagnostics, high PWM switching frequency and high-resolution audio. The high integration level and the embedded signal processing allow achieving excellent audio performances.

The HFA80A includes an I²C-bus interface to control the operation and read the state of the power amplifier, performs diagnostics and in general accesses the features reported in this datasheet.

The communication load towards the microcontroller is eased by the presence of a dedicated clipping detector and diagnostics output pin, CD/DIAG, that can trigger the host to read important information as it becomes available. All useful information derived from internal detectors (thermal warnings, output offset, overcurrent protection etc.) can in fact be selectively set to toggle the CD/DIAG pin, according to programmable configuration registers.

The HFA80A implements a new concept of load diagnostics specifically designed for automotive applications, embedding a highly reliable noise-immune load diagnostic algorithm with self-generated stimuli: this allows to detect anomalous load connections or variations and makes this information available through the I²C-bus.

4.1 Input stage

The HFA80A can work with differential or single-ended input signals. Using either has no impact on the gain of the device.

4.2 Gain selection

The HFA80A has four possible gain configurations for each channel. Each channel can be configured independently with a different gain.

4.3 Pulse-width modulator - PWM

The HFA80A channels output a modulated version of the analog input, through in-phase pulse-width modulation. Thanks to proprietary technology, this is performed with excellent stability, high bandwidth, low noise and low distortion. The PWM signal is demodulated by an external LC filter.

The choice of a high PWM switching frequency allows the use of a small-sized inductor for the demodulator filter, thus contributing to the minimization of PCB real estate occupation and cost, and makes the PWM tones lie outside the AM band, thus avoiding by design EMC interference due to the PWM harmonics.

4.4 Feedback before LC filter topology

The device works with a "feedback before the LC filter" output topology. This choice, together with the 2 MHz switching PWM, allows for the usage of smaller and cost-effective components for the demodulator filter. The HFA80A is guaranteed with a flat frequency response up to around 40 kHz, but can reach up to 80 kHz of bandwidth by tailoring the demodulator filter for this task.

4.5 Load configurations

The HFA80A supports several load configurations. The default configuration is suitable for a 4-speaker (front/rear - left/right) application. A line driver option is also available: this mode improves performance when driving high impedance loads that require a lower output current.

The maximum allowed supply voltage depends on the impedance of the loads.

4.6 Low latency

The HFA80A offers a very low latency signal processing pipeline: the delay from input analog signal to output PWM is in the order of few μ s.

This makes the HFA80A eligible for high-speed audio processing applications like noise cancelling.

4.7 Spread spectrum

Thanks to the spread spectrum feature, HFA80A is EMI-compliant according to CISPR25 up to Class V.

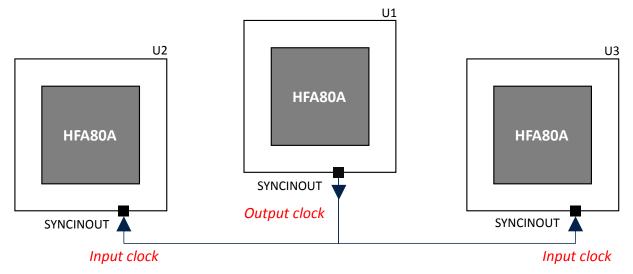
DB5280 - Rev 1 page 8/16



4.8 System clock and synchronization

The HFA80A features a synchronization pin that can be used to either receive and use a synchronization signal to generate the internal clock, or to synchronize the clock of other devices to the clock generated inside the device in question in case of multiple device applications (see the Figure 4).

Figure 4. Example of multiple channels system with synchronized clock



DB5280 - Rev 1 page 9/16

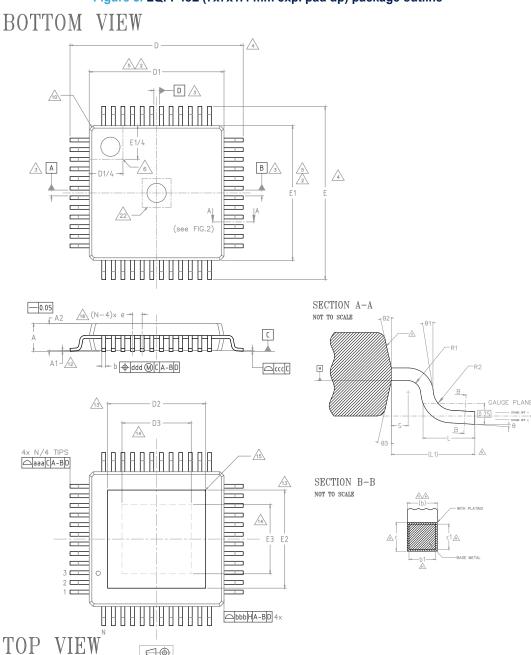


Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 LQFP48L (7x7x1.4 mm exp. pad up) package information

Figure 5. LQFP48L (7x7x1.4 mm exp. pad up) package outline



DB5280 - Rev 1 page 10/16



Table 4. LQFP48L (7x7x1.4 mm exp. pad up) package mechanical data

	Dimensions in mm			
Symbol	Min.	Тур.	Max.	
Θ	0°	3.5°	7°	
Θ1	0°	-	-	
Θ2	10°	12°	14°	
θ3	10°	12°	14°	
А	-	-	1.49	
A1	-0.03	-	0.05	
A2	1.35	1.40	1.45	
b	0.17	0.22	0.27	
b1	0.17	0.20	0.23	
С	0.09	-	0.20	
c1	0.09	-	0.16	
D		9.00 BSC		
D1		7.00 BSC		
D2	-	-	5.60	
D3	3.90	-	-	
е		0.50 BSC		
Е		9.00 BSC		
E1		7.00 BSC		
E2	-	-	5.60	
E3	3.90	-	-	
L	0.45	0.60	0.75	
L1		1.00 REF		
N		48		
R1	0.08	-	-	
R2	0.08	-	0.20	
S	0.20	-	-	
	Tolerance of form and	position		
aaa		0.20		
bbb		0.20		
ccc		0.08		
ddd		0.08		

DB5280 - Rev 1 page 11/16



Revision history

Table 5. Document revision history

Date	Revision	Changes
05-Jun-2024	1	First release.

DB5280 - Rev 1 page 12/16



Contents

1	Blo	ck diagram and pin description	3		
	1.1	Block diagram	3		
	1.2	Pin description	4		
2	App	olication schematic	6		
3	Elec	ctrical specifications	7		
	3.1	Absolute maximum ratings	7		
	3.2	Thermal data	7		
4	Gen	General description			
	4.1	Input stage	8		
	4.2	Gain selection	8		
	4.3	Pulse-width modulator - PWM	8		
	4.4	Feedback before LC filter topology	8		
	4.5	Load configurations	8		
	4.6	Low latency	8		
	4.7	Spread spectrum	8		
	4.8	System clock and synchronization	9		
5	Pac	Package information			
	5.1	LQFP48L (7x7x1.4 mm exp. pad up) package information	10		
Re	vision	history	12		
Lis	t of ta	ıbles	14		
Lis	t of fig	gures	15		



List of tables

Table 1.	Pin function	. 4
Table 2.	Absolute maximum ratings	. 7
Table 3.	Thermal data	. 7
Table 4.	LQFP48L (7x7x1.4 mm exp. pad up) package mechanical data	11
Γable 5.	Document revision history	12

DB5280 - Rev 1 page 14/16





List of figures

Figure 1.	Block diagram	. 3
Figure 2.	Device pinout	. 4
Figure 3.	Application schematic	. 6
Figure 4.	Example of multiple channels system with synchronized clock	. 9
Figure 5.	LQFP48L (7x7x1.4 mm exp. pad up) package outline	10

DB5280 - Rev 1 page 15/16



IMPORTANT NOTICE - READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2024 STMicroelectronics – All rights reserved

DB5280 - Rev 1 page 16/16