

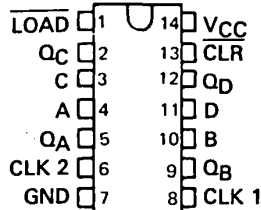
# TYPES SN54196, SN54197, SN54LS196, SN54LS197, SN54S196, SN54S197, SN74196, SN74197, SN74LS196, SN74LS197, SN74S196, SN74S197 50/30/100-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES

OCTOBER 1976 - REVISED APRIL 1985

- Performs BCD, Bi-Quinary, or Binary Counting
- Fully Programmable
- Fully Independent Clear Input
- Input Clamping Diodes Simplify System Design
- Output  $Q_A$  Maintains Full Fan-out Capability In Addition to Driving Clock-2 Input

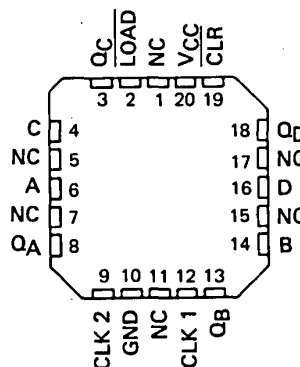
SN54196, SN54LS196, SN54S196,  
SN54197, SN54LS197, SN54S197 ... J OR W PACKAGE  
SN74196, SN74197 ... J OR N PACKAGE  
SN74LS196, SN74S196,  
SN74LS197, SN74S197 ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS196, SN54S196  
SN54LS197, SN54S197 ... FK PACKAGE  
SN74LS196, SN74S196  
SN74LS197, SN74S197 ... FN PACKAGE

(TOP VIEW)



NC - No internal connection

TYPES	GUARANTEED		TYPICAL
	COUNT FREQUENCY CLOCK 1	CLOCK 2	
'196, '197	0-50 MHz	0-25 MHz	240 mW
'LS196, 'LS197	0-30 MHz	0-15 MHz	80 mW
'S196, 'S197	0-100 MHz	0-50 MHz	375 mW

## description

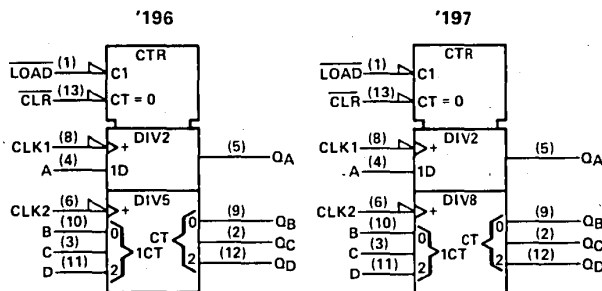
These high-speed monolithic counters consist of four d-c coupled, master-slave flip-flops, which are internally interconnected to provide either a divide-by-two and a divide-by-five counter ('196, 'LS196, 'S196) or a divide-by-two and a divide-by-eight counter ('197, 'LS197, 'S197). These four counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

All inputs are diode-clamped to minimize transmission-line effects and simplify system design. These circuits are compatible with most TTL logic families. Series 54, 54LS, and 54S circuits are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ; Series 74, 74LS, and 74S circuits are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

## logic symbols†



†Pin numbers shown on logic notation are for D, J or N packages.

**PRODUCTION DATA**  
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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**TYPES SN54196, SN54197, SN54LS196, SN54LS197, SN54S196, SN54S197,  
SN74196, SN74197, SN74LS196, SN74LS197, SN74S196, SN74S197  
50/30/100-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES**

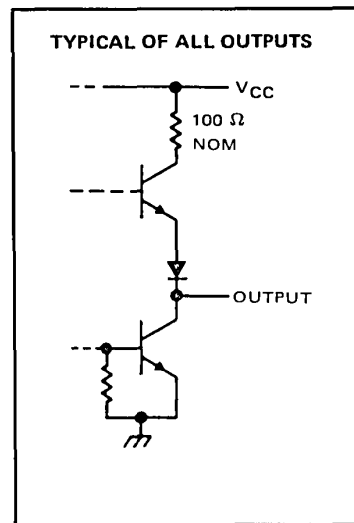
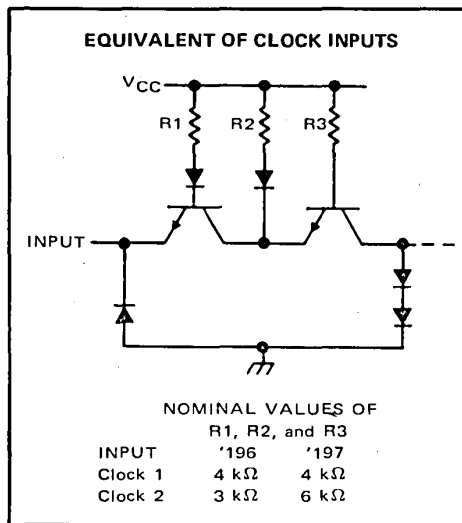
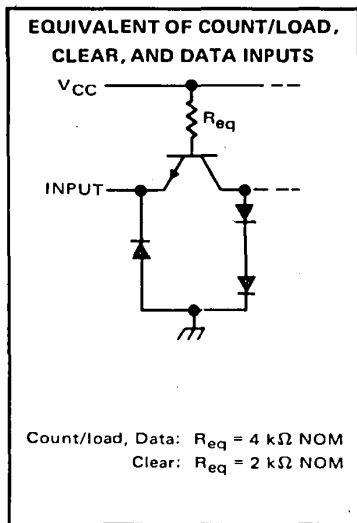
**typical count configurations**

'196, 'LS196, and 'S196 typical count configurations and function tables are the same as those for '176.  
'197, 'LS197, and 'S197 typical count configurations and function tables are the same as those for '177.

**logic diagrams**

'196, 'LS196, and 'S196 logic diagrams are the same as those for '176.  
'197, 'LS197, and 'S197 logic diagrams are the same as those for '177.

**schematics of inputs and outputs**



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## TYPES SN54196, SN54197, SN74196, SN74197 50-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54196, SN54197 Circuits	-55°C to 125°C
SN74196, SN74197 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

- NOTES: 1. Voltage values are with respect to network ground terminal.  
 2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the clear and count/load inputs.

### recommended operating conditions

		SN54196, SN54197			SN74196, SN74197			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
Supply voltage, $V_{CC}$		4.5	5	5.5	4.75	5	5.25	V		
High-level output current, $I_{OH}$		-800			-800			$\mu A$		
Low-level output current, $I_{OL}$		16			16			mA		
Count frequency	Clock-1 input	0		50	0		50	MHz		
	Clock-2 input	0		25	0		25			
Pulse width, $t_w$	Clock-1 input	10			10			ns		
	Clock-2 input	20			20					
	Clear	15			15					
	Load	20			20					
Input hold time, $t_H$	High-level data	$t_w(\text{load})$			$t_w(\text{load})$			ns		
	Low-level data	$t_w(\text{load})$			$t_w(\text{load})$					
Input setup time, $t_{SU}$ (see Note 4)	High-level data	10			10			ns		
	Low-level data	15			15					
Count enable time, $t_{EN}$ (see Note 3)		20			20			ns		
Operating free-air temperature, $T_A$		-55			125			0	70	°C

- NOTES: 3. Minimum count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.  
 4.  $t_{SU}$  is measured with respect to load input.

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TTL DEVICES

**TYPES SN54196, SN54197, SN74196, SN74197**  
**50-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES**

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54196, SN74196			SN54197, SN74197			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IH</sub> High-level input voltage		2			2			V
V <sub>IL</sub> Low-level input voltage		0.8			0.8			V
V <sub>IK</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA	-1.5			-1.5			V
V <sub>OH</sub> High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -800 μA	2.4	3.4		2.4	3.4		V
V <sub>OL</sub> Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 16 mA¶	0.2	0.4		0.2	0.4		V
I <sub>I</sub> Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V	1			1			mA
I <sub>IH</sub> High-level input current	Data, count/load	40			40			μA
	Clear, clock 1	80			80			
	Clock 2	120			80			
I <sub>IL</sub> Low-level input current	Data, count/load	-1.6			-1.6			mA
	Clear	-3.2			-3.2			
	Clock 1	-4.8			-4.8			
	Clock 2	-6.4			-3.2			
I <sub>OS</sub> Short-circuit output current §	V <sub>CC</sub> = MAX	SN54'	-20	-57	-20	-57	mA	
		SN74'	-18	-57	-18	-57		
I <sub>CC</sub> Supply current	V <sub>CC</sub> = MAX, See Note 5	48	59		48	59	mA	

NOTE 5: I<sub>CC</sub> is measured with all inputs grounded and all outputs open.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

¶Q<sub>A</sub> outputs are tested at I<sub>OL</sub> = 16 mA plus the limit value of I<sub>IL</sub> for the clock-2 input. This permits driving the clock-2 input while fanning out to 10 Series 54/74 loads.

§Not more than one output should be shorted at a time.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54196			SN54197			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f <sub>max</sub>	Clock 1	Q <sub>A</sub>	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 400 Ω, See Note 6	50	70		50	70		MHz
t <sub>PLH</sub>	Clock 1	Q <sub>A</sub>		7	12		7	12		ns
t <sub>PHL</sub>				10	15		10	15		
t <sub>PLH</sub>	Clock 2	Q <sub>B</sub>		12	18		12	18		ns
t <sub>PHL</sub>				14	21		14	21		
t <sub>PLH</sub>	Clock 2	Q <sub>C</sub>		24	36		24	36		ns
t <sub>PHL</sub>				28	42		28	42		
t <sub>PLH</sub>	Clock 2	Q <sub>D</sub>		14	21		36	54		ns
t <sub>PHL</sub>				12	18		42	63		
t <sub>PLH</sub>	A, B, C, D	Q <sub>A</sub> , Q <sub>B</sub> , Q <sub>C</sub> , Q <sub>D</sub>		16	24		16	24		ns
t <sub>PHL</sub>				25	38		25	38		
t <sub>PLH</sub>	Load	Any		22	33		22	33		ns
t <sub>PHL</sub>				24	36		24	36		
t <sub>PHL</sub>	Clear	Any		25	37		25	37		ns

◇f<sub>max</sub> ≡ maximum count frequency.

t<sub>PLH</sub> ≡ propagation delay time, low-to-high-level output.

t<sub>PHL</sub> ≡ propagation delay time, high-to-low-level output.

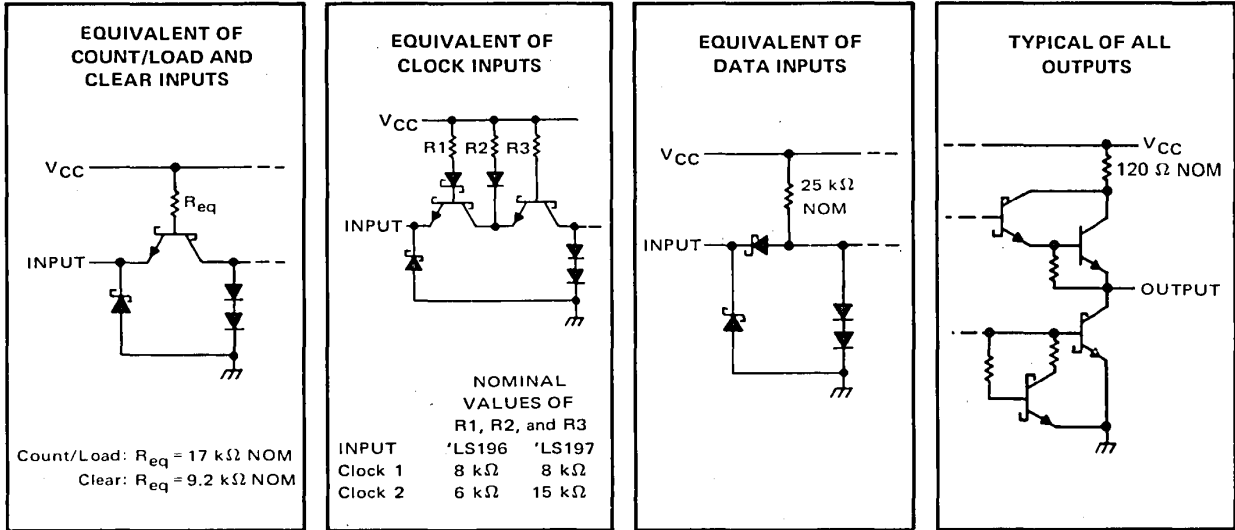
NOTE 6: Load circuit, input conditions, and voltage waveforms are the same as those shown for the '176, '177 except that testing f<sub>max</sub>, V<sub>IL</sub> = 0.3 V.



TTL DEVICES

# TYPES SN54LS196, SN54LS197, SN74LS196, SN74LS197 30-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES

## schematics of inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54LS196, SN54LS197 Circuits	-55°C to 125°C
SN74LS196, SN74LS197 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the clear and count/load inputs.

## recommended operating conditions

		SN54LS196, SN54LS197			SN74LS196, SN74LS197			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$I_{OH}$	High-level output current			-400			-400	$\mu\text{A}$
$I_{OL}$	Low-level output current			4			8	mA
	Count frequency	Clock-1 input	0	30	0	30		MHz
		Clock-2 input	0	15	0	15		
$t_w$	Pulse width	Clock-1 input	20		20			ns
		Clock-2 input	30		30			
		Clear	15		15			
		Load	20		20			
$t_h$	Input hold time	High-level data	10		10			ns
		Low-level data	10		10			
$t_{su}$	Input setup time	High-level data	10		10			ns
		Low-level data	15		15			
$t_{enable}$	Count enable time (see Note 3)	Clock 1	30		30			ns
		Clock 2	50		50			
$T_A$	Operating free-air temperature	-55		125	0		70	°C

NOTE 3: Minimum count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.



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**TYPES SN54LS196, SN54LS197, SN74LS196, SN74LS197**  
**30-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES**

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS196 SN54LS197			SN74LS196 SN74LS197			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage		0.7			0.8			V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA	-1.5			-1.5			V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> max, I <sub>OH</sub> = -400 µA	2.5	3.4		2.7	3.4	V	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> max	I <sub>OL</sub> = 4 mA†		0.25	0.4	0.25	0.4	V
			I <sub>OL</sub> = 8 mA†				0.35	0.5	
I <sub>I</sub>	Input current at maximum input voltage	Data, count/load Clear, clock 1 Clock 2 of 'LS196 Clock 2 of 'LS197	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V				0.1		0.1
							0.2		0.2
							0.4		0.4
							0.2		0.2
I <sub>IH</sub>	High-level input current	Data, count/load Clear, clock 1 Clock 2 of 'LS196 Clock 2 of 'LS197	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V				20		20
							40		40
							80		80
							40		40
I <sub>IL</sub>	Low-level input current	Data, count/load Clear Clock 1 Clock 2 of 'LS196 Clock 2 of 'LS197	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V				-0.4		-0.4
							-0.8		-0.8
							-2.4		-2.4
							-2.8		-2.8
							-1.3		-1.3
I <sub>OS</sub>	Short-circuit output current‡	V <sub>CC</sub> = MAX	-20	-100	-20	-100	mA		
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = MAX, See Note 4	16	27	16	27	mA		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

¶ Q<sub>A</sub> outputs are tested at specified I<sub>OL</sub> plus the limit value of I<sub>IL</sub> for the clock-2 input. This permits driving the clock-2 input while maintaining full fan-out capability.

NOTE 4: I<sub>CC</sub> is measured with all inputs grounded and all outputs open.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER <sup>◇</sup>	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54LS196 SN74LS196			SN54LS197 SN74LS197			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f <sub>max</sub>	Clock 1	Q <sub>A</sub>	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ, See Note 5	30	40		30	40	MHz	
t <sub>PLH</sub>	Clock 1	Q <sub>A</sub>		8	15		8	15	ns	
t <sub>PHL</sub>				13	20		14	21		
t <sub>PLH</sub>	Clock 2	Q <sub>B</sub>		16	24		12	19	ns	
t <sub>PHL</sub>				22	33		23	35		
t <sub>PLH</sub>	Clock 2	Q <sub>C</sub>		38	57		34	51	ns	
t <sub>PHL</sub>				41	62		42	63		
t <sub>PLH</sub>	Clock 2	Q <sub>D</sub>		12	18		55	78	ns	
t <sub>PHL</sub>				30	45		63	95		
t <sub>PLH</sub>	A, B, C, D	Q <sub>A</sub> , Q <sub>B</sub> , Q <sub>C</sub> , Q <sub>D</sub>		20	30		18	27	ns	
t <sub>PHL</sub>				29	44		29	44		
t <sub>PLH</sub>	Load	Any		27	41		26	39	ns	
t <sub>PHL</sub>				30	45		30	45		
t <sub>PHL</sub>	Clear	Any		34	51		34	51	ns	

◇ f<sub>max</sub> ≡ maximum count frequency

t<sub>PLH</sub> ≡ propagation delay time, low-to-high-level output, t<sub>PHL</sub> ≡ propagation delay time, high-to-low-level output

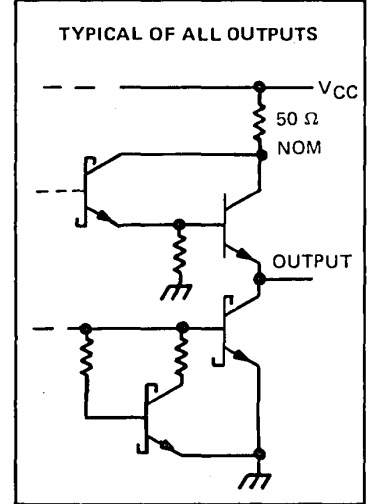
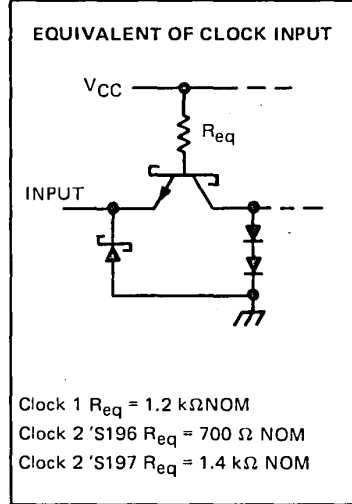
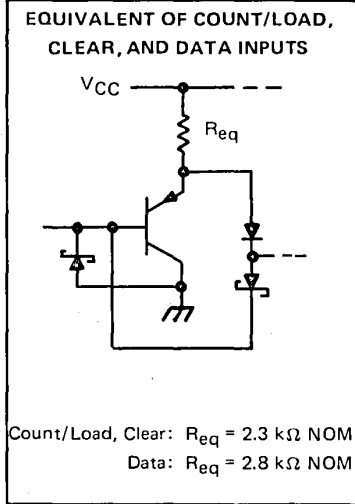
NOTE 5: Load circuit, input conditions, and voltage waveforms are the same as those shown for the '176, '177 except that t<sub>r</sub> ≤ 15 ns, t<sub>f</sub> ≤ 6 ns, and V<sub>ref</sub> = 1.3 V (as opposed to 1.5 V)

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TTL DEVICES

# TYPES SN54S196, SN54S197, SN74S196, SN74S197 100-MHz PRESETTABLE DECADE AND BINARY COUNTERS/LATCHES

## schematics of inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54S196, SN54S197 Circuits	-55°C to 125°C
SN74S196, SN74S197 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

		SN54S196, SN54S197			SN74S196, SN74S197			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$		4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$					-1			mA
Low-level output current, $I_{OL}$					20			mA
Clock frequency	Clock-1 input	0		100	0		100	MHz
	Clock-2 input	0		50	0		50	
Pulse width, $t_w$	Clock-1 input	5			5			ns
	Clock-2 input	10			10			
	Clear	30			30			
	Load	5			5			
Input hold time, $t_h$	High-level data	3 $\uparrow$			3 $\uparrow$			ns
	Low-level data	3 $\uparrow$			3 $\uparrow$			
Input setup time, $t_{SU}$ (see Note 6)	High-level data	6 $\uparrow$			6 $\uparrow$			ns
	Low-level data	6 $\uparrow$			6 $\uparrow$			
Count enable time, $t_{eN}$ (see Note 2)		12			12			ns
Operating free-air temperature, $T_A$		-55		125	0		70	°C

NOTES: 2. Minimum count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs are both high to permit counting.

6.  $t_{SU}$  is measured with respect to load input.

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TTL DEVICES

# TYPES SN54S196, SN54S197, SN74S196, SN74S197

## 100-MHz PRESETTABLE DECADE AND BINARY COUNTERS/LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †		SN54S196, SN74S196			SN54S197, SN74S197			UNIT
			MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V <sub>IH</sub>			2			2			V
V <sub>IL</sub>			0.8			0.8			V
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA		-1.2			-1.2			V
V <sub>OH</sub>		V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -1 mA	54S	2.5	3.4	2.5	3.4	V	
			74S	2.7	3.4	2.7	3.4		
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 20 mA ¶		0.5			0.5			V
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V		1			1			mA
I <sub>IH</sub>	Clock 1, clock 2	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V	150			150			µA
	All other inputs		50			50			
I <sub>IL</sub>	Data, count/load Clear	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V	-0.75			-0.75			mA
	Clock 1		-8			-8			mA
	Clock 2		-10			-6			mA
I <sub>OS</sub> §	V <sub>CC</sub> = MAX		-30	-110	-30	-110	mA		
I <sub>CC</sub>	V <sub>CC</sub> = MAX, See Note 3		54S	75	110	75	110	mA	
			74S	75	120	75	120		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

¶ Q<sub>A</sub> outputs are tested at I<sub>OL</sub> = 20 mA plus the limit value of I<sub>IL</sub> for the clock-2 input. This permits driving the clock-2 input while fanning out to 10 Series 54S/74S loads.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 3: I<sub>CC</sub> is measured with all inputs grounded and all outputs open.

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TTL DEVICES

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER ◊	(FROM (INPUT))	TO (OUTPUT)	TEST CONDITIONS	SN54S196, SN74S196			SN54S197, SN74S197			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f <sub>max</sub>	Clock 1	Q <sub>A</sub>	R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 15 pF, See Note 4	100	140		100	140		MHz
t <sub>PLH</sub>	Clock 1	Q <sub>A</sub>		5	10		5	10		ns
t <sub>PHL</sub>				6	10		6	10		
t <sub>PLH</sub>	Clock 2	Q <sub>B</sub>		5	10		5	10		ns
t <sub>PHL</sub>				8	12		8	12		
t <sub>PLH</sub>	Clock 2	Q <sub>C</sub>		12	18		12	18		ns
t <sub>PHL</sub>				16	24		15	22		
t <sub>PLH</sub>	Clock 2	Q <sub>D</sub>		5	10		18	27		ns
t <sub>PHL</sub>				8	12		22	33		
t <sub>PLH</sub>	A,B,C,D	Q <sub>A</sub> ,Q <sub>B</sub> ,Q <sub>C</sub> ,Q <sub>D</sub>		7	12		7	12		ns
t <sub>PHL</sub>				12	18		12	18		
t <sub>PLH</sub>	Load	Any		10	18		10	18		ns
t <sub>PHL</sub>				12	18		12	18		
t <sub>PHL</sub>	Clear	Any		26	37		26	37		ns

◊ f<sub>max</sub> = maximum input counting frequency.

t<sub>PLH</sub> = propagation delay time, low-to-high-level output.

t<sub>PHL</sub> = propagation delay time, high-to-low-level output.

NOTE 4: See General Information Section for load circuits and voltage waveforms.