TYPES SN74LS462, SN74LS463
FIBER-OPTIC DATA-LINK CONTROLLERS

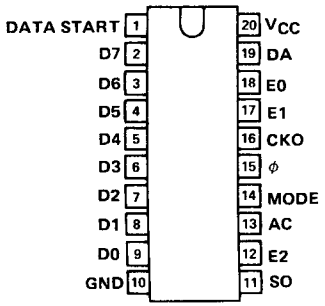
AUGUST 1979

- Inexpensive, Reliable Alternative to Conventional Copper-Wire Systems
- Single 5-Volt Supply
- Inputs and Outputs Compatible with TTL and Low-Level MOS
- Data Rate of 1 Megabit/Second
- Byte-Oriented Expansion Capability for 16-Bit Applications
- Interfaces With a Wide Range of Optical-Link Components
- Space-Saving 20-Pin 300-Mil Package

SN74LS462 TRANSMITTER

- Drive Current Up To 200 mA
- Three Operational Modes:
  - Continuous Data Stream
  - DC Sync (8-Bit or 16-Bit Bursts)
  - AC Sync (8-Bit or 16-Bit Bursts)
- Automatic Start-Up

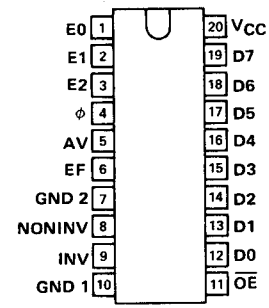
SN74LS462
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



SN74LS463 RECEIVER

- Input Sensitivity of 1 μA
- Error Indication
- 3-State Parallel Data Outputs
- Isolated Comparator Ground For Improved Common-Mode Noise Rejection

SN74LS463
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The SN74LS462 transmitter and SN74LS463 receiver are designed for use in optical-wave data-transmission systems. Fabricated with oxide-isolated Integrated Injection Logic (I^2L) and low-power Schottky† TTL technology, these devices are operated from a single 5-volt dc power source and are completely TTL-compatible on all inputs and outputs. The SN74LS462/SN74LS463 transmitter/receiver pair are designed to provide the appropriate encoding, synchronizing, and decoding logic necessary control the transmission of digital data through a wide variety of serial fiber-optic data-link assemblies.

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† Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

description (continued)

The basic fiber-optic data link shown in Figure 1 consists of five stages; encoding logic, which converts parallel data to be transmitted into a modulated serial data stream; a transducer (source) to convert the electrical serial data stream into optical logic levels (LED on or off); an optical waveguide (fiber) for transmission of the optical data stream; a transducer (detector), which converts the optical levels back into electrical logic levels; and lastly, decoding logic to convert the modulated serial data stream back into parallel output data.

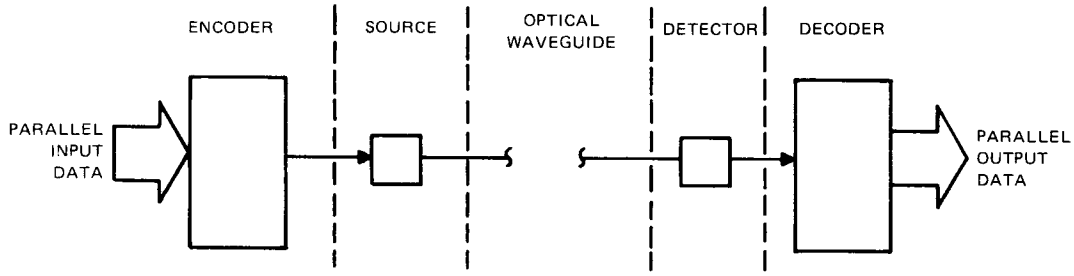


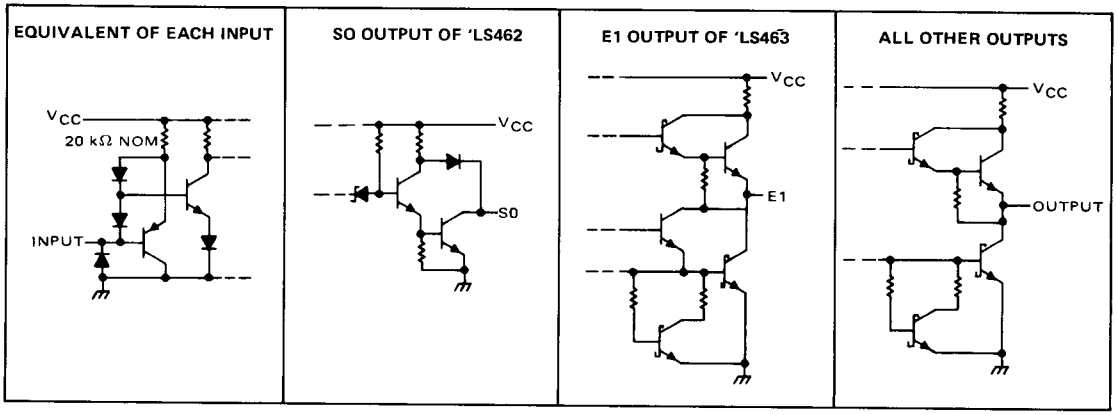
FIGURE 1 – TYPICAL SIMPLEX FIBER-OPTIC DATA LINK

The functions of encoding and decoding are efficiently provided by the SN74LS462 transmitter and SN74LS463 receiver, respectively, by incorporating all of the necessary logic in space-saving, 20-pin, 300-mil packaging. Transducer functions and transmission fibers can be selected from a wide variety of plastic, glass, or silica assemblies now available including Texas Instruments TXE series of low-cost, all plastic, source, detector, and fiber-cable assemblies.

The SN74LS462 transmitter accepts eight-bit parallel data inputs, encodes this data into frequency-shift coding (FSC), and transmits this information in the user-selected operating mode out of the serial output. (For an explanation of frequency-shift coding, see the "Operation" section of this data sheet). The serial output is capable of driving directly an infrared-emitting diode (IRED), which is coupled through a fiber-optic cable to a PIN detector diode. The SN74LS463 receiver then accepts very low-level currents from the PIN detector into an internal transimpedance amplifier, which amplifies this signal to the level required by the logic. The receiver then decodes the serial data stream and reconstructs the eight bits of parallel data originally transmitted. The parallel data word may be expanded to 16-bits through the addition of four standard low-power Schottky components interfaced to the transmitter's and receiver's expand pins. Both transmitter and receiver require either a crystal or TTL-level clock connected to the ϕ input.

More detailed information on the functions of these controllers is included elsewhere in this data sheet in the section entitled "Operation".

schematics of inputs and outputs



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SN74LS462

PIN	SIGNATURE	FUNCTION
1	DS	Data start input loads data into the buffer register on the low-to-high-level transition provided that the data acknowledge output is high.
2	D7	Parallel data inputs.
3	D6	
4	D5	
5	D4	
6	D3	
7	D2	
8	D1	
9	D0	
10	GND	Ground.
11	SO	Serial output provides a signal capable of driving an infrared-emitting diode (200 mA maximum). SO is connected to the cathode of the diode, and the anode is connected to five volts through a 33-ohm resistor.
12	E2	Expand-2 input accepts inverted data from an external eight-bit shift register for 16-bit operation.
13	AC	AC sync input, which, if mode input is high, selects the AC mode of operation when high and the DC mode when low.
14	MODE	Mode input when high allows the AC input to select either AC sync mode or DC sync mode. When low (and AC is low), it selects the continuous mode of operation.
15	ϕ	Clock input for crystal or TTL clock. (Clock frequency = 8X data rate).
16	CKO	Clock output provides clock frequency to the receiver at the same location when bidirectional operation is required.
17	E1	Expand-1 output shifts data out of the external shift register for 16-bit operation. For eight-bit operation this is an input and it must be high.
18	E0	Expand-0 output loads external serial shift register for 16-bit operation.
19	DA	Data-acknowledge output provides a signal that, when high, indicates that the buffer register is ready to accept data. It goes low approximately 250 ns after a low-to-high-level transition of data start thereby acknowledging the input of data.
20	V_{CC}	+5V Supply.

SN74LS463

PIN	SIGNATURE	FUNCTION
1	E0	Expand-0 output supplies serial data to an external shift register for 16-bit operation.
2	E1	Expand-1 output supplies a clock signal to an external serial shift register for 16-bit operation. For eight-bit operation this is an input and should be shorted to V_{CC}.
3	E2	Expand-2 output provides a signal to load data from the external serial register to the external parallel-output buffer register for 16-bit operation.
4	ϕ	Clock input for crystal or TTL clock. (Clock frequency = 8X data rate).
5	AV	Data-available output goes high when a demodulated word is transferred from the serial shift register to the parallel-output buffer register. This output is self-clearing: it goes inactive (low) typically 800 nanoseconds after going high.
6	EF	Error-flag output goes high if a data bit times out during the transmission of 8 or 16 bits of data; that is, if an FSC transition has not occurred in 10 clock periods. It will then remain high (and AV will be inhibited [low]) until 8 bits (or 16 bits for 16-bit operation) have been received without a time-out error occurring on any bit.
7	GND2	Comparator ground.
8	NONINV	Noninverting comparator input from the infrared-detecting diode.
9	INV	Inverting comparator input from the infrared-detecting diode.
10	GND1	Digital ground.
11	$\overline{OE}$	Output enable input, which, when low, enables the buffer register outputs and when high, forces the buffer register outputs into the high-impedance state.
12	D0	Buffer register data outputs.
13	D1	
14	D2	
15	D3	
16	D4	
17	D5	
18	D6	
19	D7	
20	V_{CC}	+5 V Supply.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, any logic input . . . . . 7 V
Off-state output voltage, SN74LS463 data outputs . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN74LS462			SN74LS463			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.25	4.75	5	5.25	V
Off-state output voltage, SN74LS463 data outputs							5.5	V
High-level output voltage, SO output				5.5				V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}	SO output			200				mA
	E1 output						3	
	other outputs			8			8	
Operating free-air temperature, T_A		0		70	0		70	°C

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN74LS462			SN74LS463			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level logic input voltage				2			2			V
V_{IL}	Low-level logic input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_T	Comparator input threshold voltage		V_{CC} = MAX						1.2		V
	Comparator input current		V_{CC} = MAX					1		100	μA
V_{OH}	High-level output voltage (any output except SO)		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = 0.4 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	SO output	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5				V
		E1 output				0.35	0.5		0.35	0.5	
		other outputs				0.35	0.5		0.35	0.5	
I_{OH}	High-level output current, (SO output)		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V			4				mA
I_{OZH}	Off-state output current, high-level voltage applied (D0-D7 outputs)		V_{CC} = MAX, V_O = 2.7 V	V_{IH} = 2 V,						50	μA
I_{OZL}	Off-state output current, low-level voltage applied (D0-D7 outputs)		V_{CC} = MAX, V_O = 0.4 V	V_{IH} = 2 V,						−50	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V						1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.4 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX				100			100	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

timing requirements over recommended ranges of T_A and V_{CC}

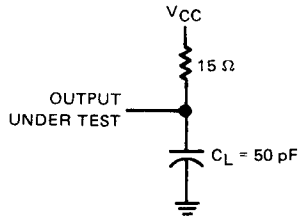
PARAMETER		SN74LS462			SN74LS463			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(\phi)}$	Clock cycle time	100			100			ns
$t_{r(\phi)}$	Clock rise time						18	ns
$t_{f(\phi)}$	Clock fall time		9				18	ns
$t_{w(\phi)}$	Clock pulse width	50			50			ns
t_{su}	Setup time, data in before data start	15						ns
t_h	Hold time, data in after data start	30						ns

switching characteristics over recommended ranges of T_A and V_{CC}

PARAMETER		TEST CONDITIONS	SN74LS462			SN74LS463			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_d	Delay time, data start high to data acknowledge low	See Figures 2 and 3		450					ns
t_d	Delay time, data in to serial out			250					ns
t_d	Delay time, output enable to data out						35		ns
t_d	Delay time, data in to data available							400	ns
t_d	Delay time, invalid data to error flag							300	ns
t_d	Delay time, clock (ϕ) input to clock output			30					ns
t_w	Pulse width, data available high							800	ns

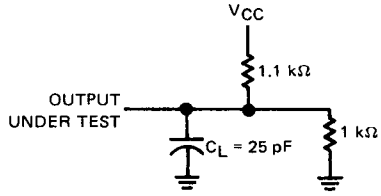
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



C_L includes probe and jig capacitance

SN74LS462 LOAD CIRCUIT



C_L includes probe and jig capacitance

SN74LS463 LOAD CIRCUIT

FIGURE 2 – LOAD CIRCUITS

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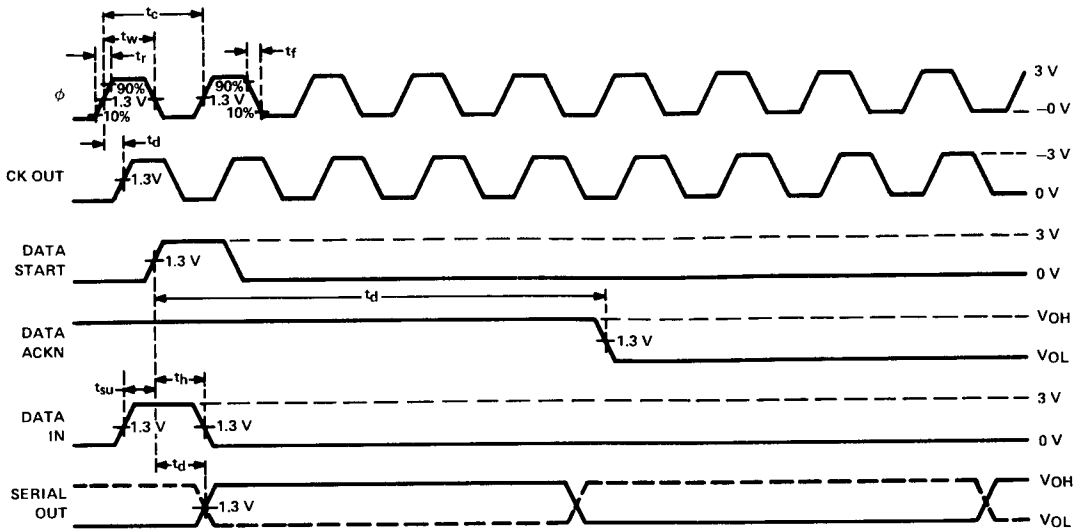
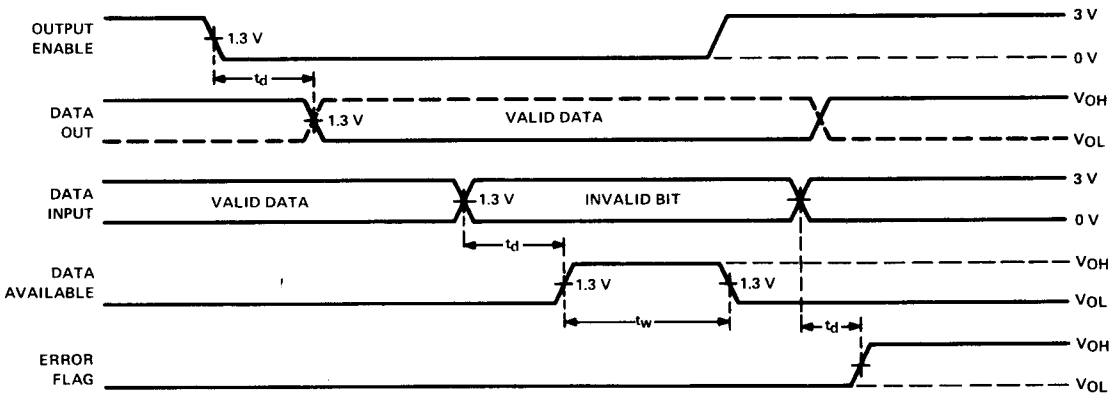
PARAMETER MEASUREMENT INFORMATION



SN74LS462 VOLTAGE WAVEFORMS



SN74LS463 VOLTAGE WAVEFORMS

FIGURE 3 – SWITCHING CHARACTERISTICS

OPERATION

serial data coding and synchronization

frequency-shift coded (FSC) data

Frequency-shift coding, or FSC, is a term for a data transmission code in which each bit period begins with a transition. A space ('0') has no transition during the bit period, however, a mark ('1') has one transition during the bit period (See Figure 4). FSC formatting provides the advantage that it is self-clocking and therefore precludes the necessity of transmitting a clock signal to the receiving end to define the point in time in which data is valid. The SN74LS462 transmitter and SN74LS463 receiver incorporate FSC data to provide a data rate of one megabit per second.

FIGURE 4—FSC SERIAL DATA

continuous-data-stream mode

Continuous-data-stream mode refers to a mode of serial data transmission in which the word boundaries between consecutive transmissions are not defined by any type of synchronization periods. (See Figure 5A). That is, the next consecutive word is transmitted immediately following the previous word. When no further data is to be transmitted, the serial data line goes to a logic high (LED off) state until a new word is to be transmitted. Continuous data stream offers the advantage of a higher data rate than synchronized transmission schemes.

dc-synchronization mode

In the dc-synchronization mode, word boundaries are separated by two bit times at a high logic level (LED off). When no data is to succeed the previous transmission, the serial data line goes to a logic high state until a new word is to be transmitted (See Figure 5B). When new data is to be transmitted after an extended (greater than two bit times) idle period, the current synchronization period will be completed prior to transmission. (i.e., idle periods are always a multiple of two bit time sync periods). Dc synchronization offers the advantage over continuous data stream in that word boundaries are defined by the synchronization period.

ac-synchronization mode

Ac synchronization refers to a three-bit time synchronization period wherein the signal is low for one half of the synchronization period (one and a half bit times) and is high for the other half of the synchronization period. The initial state of the synchronization period is dependent upon the status of the serial data line when the synchronization period is entered. If the serial line is low, the first half of the synchronization period is high and the second half is low. Likewise, if the serial line is high, the first half of the synchronization period is low and the second half is high. When no further data is to succeed the previous transmission, the alternating synchronization period is repeated until the next word is to be transmitted. The current synchronization period will be completed prior to data transmission. (See Figure 5C). Ac synchronization provides the advantage that the receiving end remains in constant synchronization with the transmitting end, even during extended idle periods.

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OPERATION

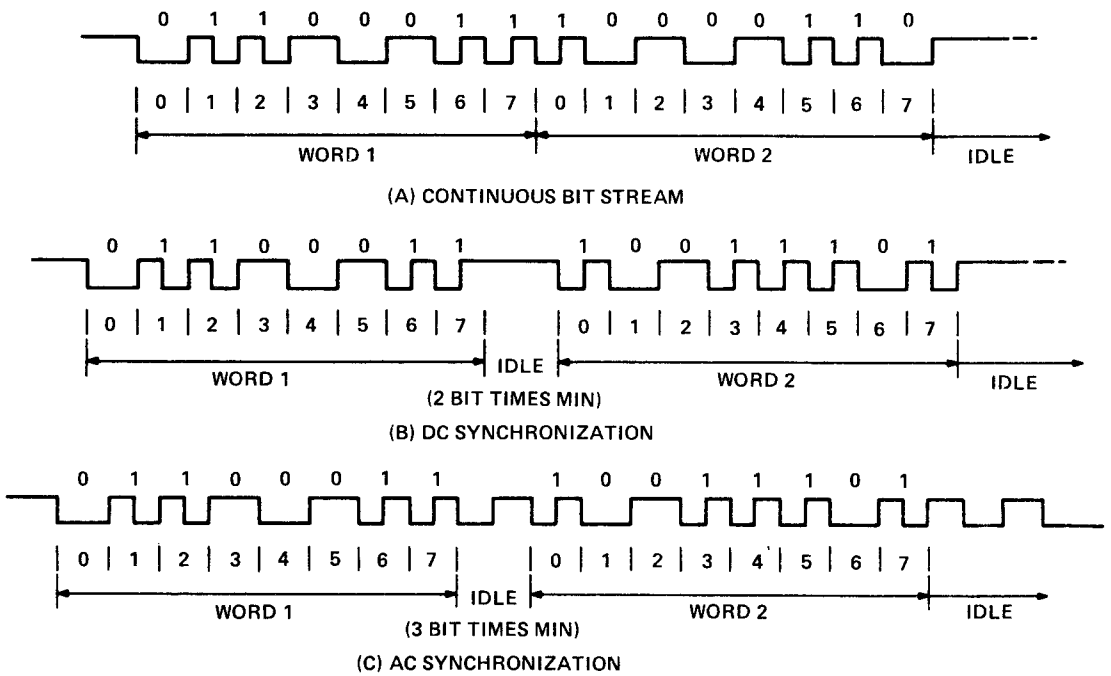

FIGURE 5 – SN74LS462 TRANSMITTER MODES OF OPERATION

SN74LS462 transmitter functional description

SN74LS462 operational description

When power is first applied to the transmitter, power-up circuitry causes the data acknowledge (DA) output to go active (high) indicating that the buffer register is empty and ready to accept data. (See Figure 6). Parallel loading of the data present on the D0-D7 input pins is accomplished by taking the data start (DS) input high when the data acknowledge is high. Loading will then occur on the rising edge of data start. The parallel data loaded into the buffer register appears at the inputs of the shift register. Approximately 250 nanoseconds after the rising edge of data start, data acknowledge (DA) goes inactive (low). Simultaneously, control logic sends out a pulse to the shift register, and the shift register loads the data from the buffer register. After this operation is complete, data acknowledge once again goes active (high) to indicate that the buffer register is ready to accept new data. The new data now present on the D0-D7 data lines will be entered into the buffer register upon the occurance of the next low-to-high transition of data start. The shift register begins shifting data, one bit at a time, into the modulator where it is encoded into FSC format and output on the serial output (SO) pin. After the eighth bit has been transmitted, further operation depends upon the mode of operation selected by the MODE and ac-sync (AC) inputs. (See Table 1). If the continuous-data-stream mode is selected, the next eight bits are loaded into the shift register from the buffer register and shifting of the data continues without interruption. In the dc-sync mode, the two-bit synchronization period will be inserted between consecutive transmissions. In the

OPERATION

ac-sync mode, the three-bit synchronization period will be inserted between consecutive transmissions. (See ac-synchronization mode.) In all modes, the output of the modulator is amplified so that the serial output (SO) is capable of directly driving an external infrared-emitting diode (source).

In all modes, if the buffer and shift registers are empty, data acknowledge will be high and the transmitter will enter the wait mode. In the wait mode, if dc-sync or continuous (bit stream) operation is selected, the SO output will remain high (transmit diode off). In the ac-sync mode, the SO output will repeat the three-bit synchronization period. The wait mode is ended by the rising edge of a data start pulse. When exiting an extended wait period, the transmitter will complete the current synchronization period (two bit times for dc-sync, three bit times for ac-sync) prior to beginning serial output from SO.

The transmitter has a clock input (ϕ) for connection of crystal or TTL-level clock. The bit time is defined as eight cycles of the clock input so that for one-megabit-per-second operation, the clock (ϕ) frequency must be 8 megahertz. The clock output (CKO) may be used to source the SN74LS463 receiver clock input when full-duplex (bidirectional) systems are configured. The two expander outputs, E0 and E1, and the expander input E2 are used to control external devices when the transmitter is configured for 16-bit operation (see Figure 7). However, for 8-bit operation E1 must be tied directly to V_{CC} (+5 volts).

FUNCTION TABLE

INPUTS		SYNC SELECTED
MODE (PIN 14)	AC (PIN 13)	
L	L	Continuous (no sync)
L	H	Undefined
H	L	DC sync
H	H	AC sync

H = high level, L = low level

TABLE 1 – MODE-SELECT FUNCTION TABLE

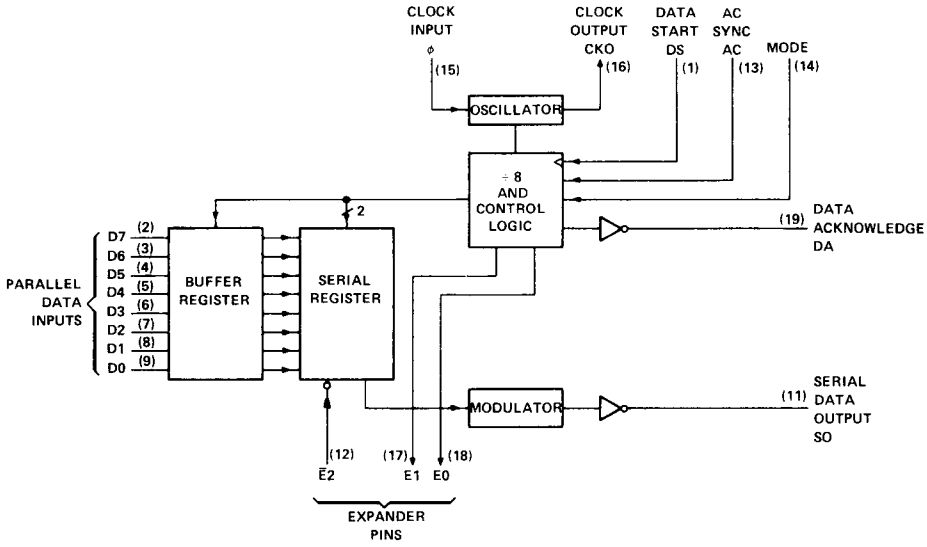

FIGURE 6–SN74LS462 FUNCTIONAL BLOCK DIAGRAM

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SN74LS462 transmitter 16-bit expansion

Sixteen-bit expansion of the transmitter is effected through connection of an SN74LS377 octal D-type flip-flop and an SN74LS165 octal shift register to the expander pins of the transmitter (E0, E1, and E2). (See Figure 7). Addition of these two standard low-power Schottky devices effectively expands the buffer and shift registers of the transmitter to 16 bits. Input E2 is the serial data output of the 'LS165. Outputs E0 and E1 control the shift/load and clock functions, respectively, of the 'LS165. Note that the data start (DS) input is also used to clock data into the 'LS377 external buffer register. Operation in 16-bit mode is identical to 8-bit operation except that the transmitted word length is now 16-bits long.

source interface to SN74LS462 transmitter

The serial output (SO) of the transmitter utilizes extremely large output buffer circuitry to provide 200 milliamperes of low-level sink current. This allows the SN74LS462 transmitter to be interfaced to a wide variety of infrared emitting diode (IRED) source assemblies.

The source assembly is connected in the manner illustrated in Figure 8. Note that for a forward diode current of 100 milliamperes, resistor R is shown to be 32 ohms.

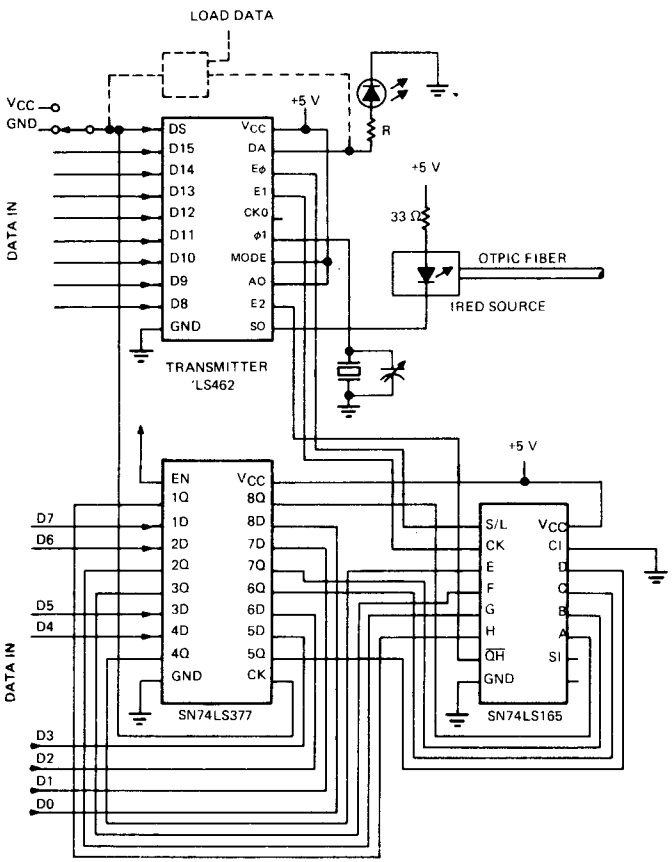

FIGURE 7 – SN74LS462 16-BIT CONFIGURATION

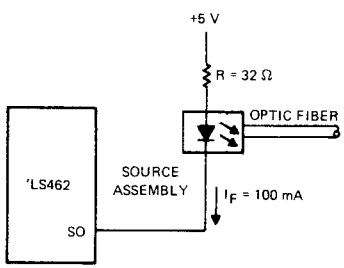

FIGURE 8 – SOURCE ASSEMBLY CONNECTION TO SN74LS462

OPERATION

SN74LS463 receiver functional description

SN74LS463 operation description

The SN74LS463 receiver receives very-low-level currents generated by the external photodiode detector, amplifies this signal, and decodes it into eight (or optionally 16) parallel data outputs. A block diagram of the SN74LS463 is shown in Figure 9.

The SN74LS463 has amplifier/comparator inputs, NONINV and INV, which receive the signal from the photodetector. The clock input (ϕ) provides the synchronization for the circuit. The error flag (EF) output indicates a long-bit error has occurred during the transmission of the eight (or 16) bits of data. The data available output (AV) indicates when the data is available at the output buffer register (D0-D7). The AV output will remain active (high) until the occurrence of an appropriate edge is received by the receiver. For the ac-sync mode, AV will clear typically 800 nanoseconds after it becomes active. For the continuous and dc-sync modes, the time at which AV is cleared inactive (low) is dependent upon the state of the input when the last bit of a bit stream is received. If the bit stream is concluded with a high logic level, the next input transition that clears AV will not occur until the first transition of the first bit of the next eight (or 16) bits to be received. However, if the bit stream is concluded with a low logic level, AV will be cleared when the transition to the high logic level of idle is entered. Because the actual point when AV becomes inactive (low) is dependent upon the subsequent data transmitted system designers are urged to utilize the rising edge of AV to set flags, control logic, etc. in their systems. The output enable ($\overline{OE}$) input either enables the eight parallel three-state outputs or forces them into the high-impedance state. The expander outputs, E0, E1, and E2, are used to expand receiver operation to 16 bits. For eight-bit operation, E1 must be connected to V_{CC}.

The first stage of the SN74LS463 is a low-noise front-end amplifier optimized for use with a PIN detector diode. When the photodiode detects the infrared signal transmitted through the fiber-optic cable, it produces an output current proportional to the received infrared intensity. This current is converted to a voltage by the comparator transimpedance amplifier and amplified to the levels required for internal logic. The FSC information synchronizes with the timer-counter logic in the demodulator where it is demodulated into non-return-to-zero (NRZ) format and fed to a serial shift register. The internal shift register accepts eight-bit serial data and transfers it in parallel to the buffer register. The data outputs from the buffer register are controlled by the output enable ($\overline{OE}$) input; a low at this input enables the outputs, a high forces the outputs to the high-impedance state. If 16-bit operation is selected, serial data will shift out through output E0 to the serial input of an external shift register and data from the external shift register is loaded

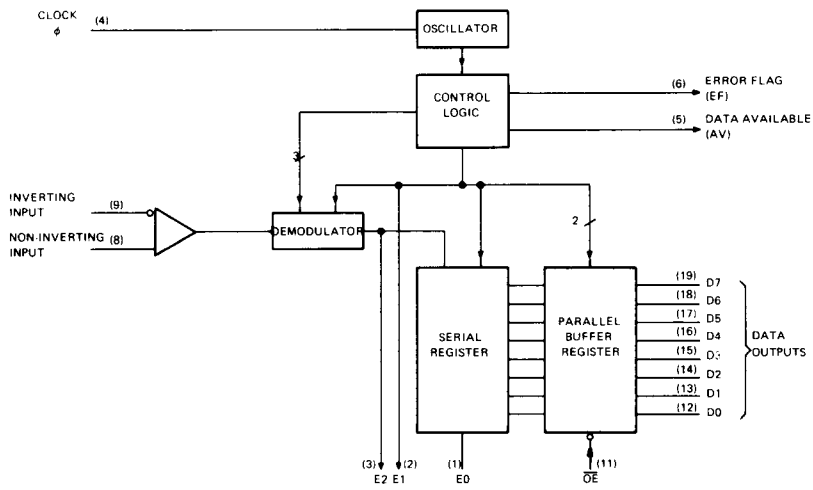

FIGURE 9 – SN74LS463 FUNCTIONAL BLOCK DIAGRAM

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OPERATION

into an external buffer register with a pulse from output E2. A clock signal is supplied to the external shift register through output E1, but for eight-bit operation E1 acts as an input and must be tied to V_{CC}.

The receiver counts eight clock pulses for each data bit. If an FSC transition has not occurred within ten clock periods, the bit will time-out. If less than eight bits (or 16 bits for 16-bit operation) have been received when a time-out error occurs, data available will be inhibited (low) and error flag will go high until eight bits (or 16 bits for 16-bit operation) have been received without a time-out error occurring on any bit. After eight bits (or 16 bits for 16-bit operation) have been received without a time-out error, error flag will go low and data available will operate normally. At the end of each eight bits (or 16 bits), a two-bit or longer synchronization pulse (idle period) may occur. This will be recognized as such by the internal circuitry, and error flag will remain low. If synchronization pulses do not occur after eight bits (or 16 bits for 16-bit operation), the continuous bit-stream mode will be assumed.

SN74LS463 receiver 16-bit expansion

Sixteen-bit expansion of the receiver is effected through connection of an SN74LS164 8-bit serial shift register and an SN74LS374 octal D-type flip-flop to the expander pins of the receiver (E0, E1, and E2). Figure 10 illustrates the connection of these devices to the receiver.

detector interface to the SN74LS463 receiver

The detector assembly is connected to the receiver in the manner illustrated in Figure 11. The PIN detector diode is connected to the NONINV comparator input, and the second diode is a compensating diode connected to the INV comparator input to offset the effects of temperature on the PIN diode characteristics and to establish a PIN "dark" low-level current level.

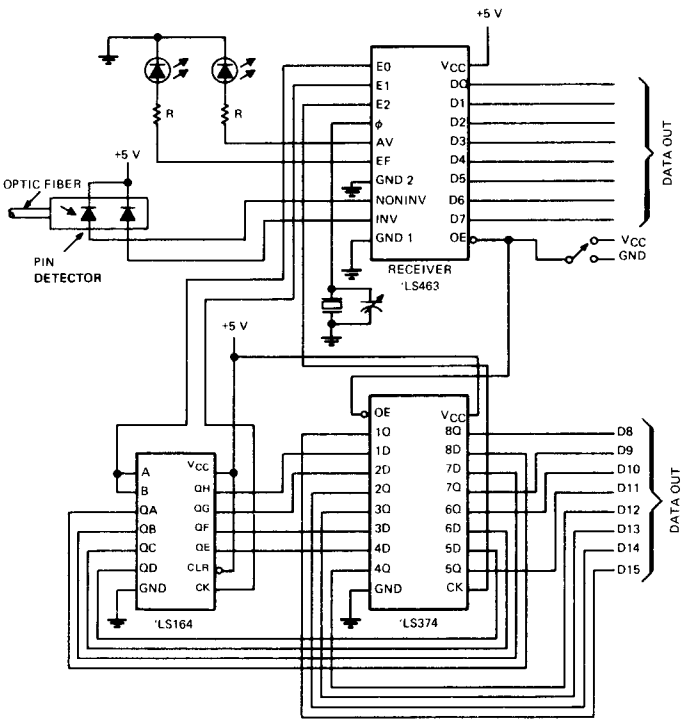

FIGURE 10 – SN74LS463 16-BIT CONFIGURATION

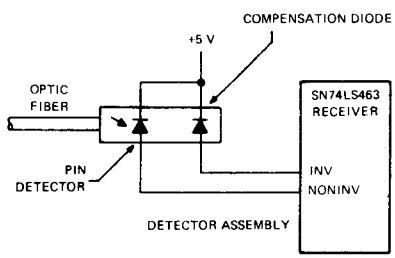

FIGURE 11 – DETECTOR ASSEMBLY CONNECTION TO SN74LS462

OPERATION

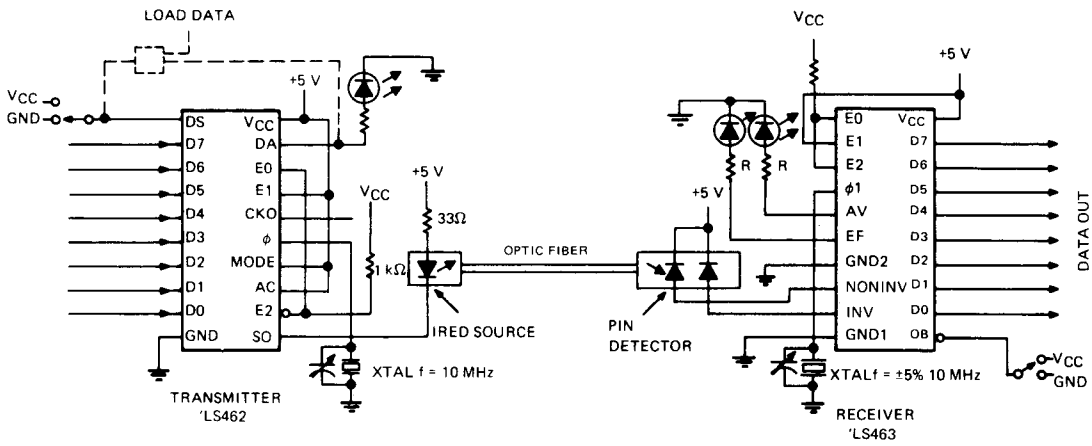

FIGURE 12 – WIRING DIAGRAM 8-BIT AC SYNC MODE

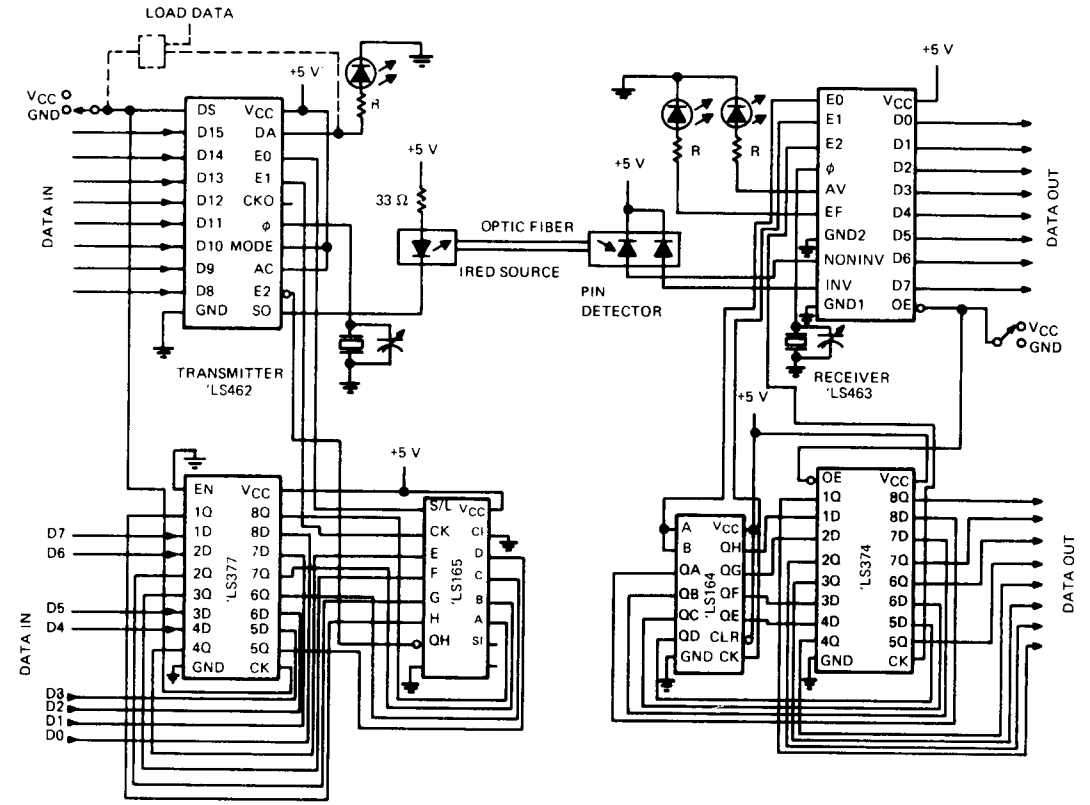

FIGURE 13 – WIRING DIAGRAM 16-BIT AC SYNC MODE

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