

TYPES SN54LS440 THRU SN54LS444, SN54LS448 SN74LS440 THRU SN74LS444, SN74LS448 QUADRUPLE TRIDIRECTIONAL BUS TRANSCEIVERS

D2425, AUGUST 1979

- 3-Way Asynchronous Communication
- On-Chip Bus Selection Decoding
- Input Hysteresis Improves Noise Margin
- Choice of Open-Collector or 3-State Outputs

description

These bus transceivers are designed for asynchronous three-way communication between four-line data buses. They give the designer a choice of selecting inverting, noninverting, or a combination of inverting and noninverting data paths with either 3-state or open-collector outputs.

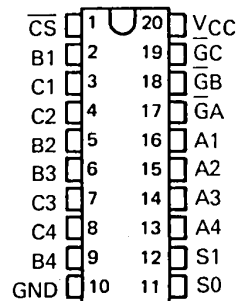
The S0 and S1 inputs select the bus from which data are to be transferred. The G inputs enable the bus or buses to which data are to be transferred. The port for any bus selected for input and any other bus not enabled for output will be at high impedance including those of the open-collector devices.

The SN54LS440 through SN54LS444 and SN54LS448 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS440 through SN74LS444 and SN74LS448 are characterized for operation from 0°C to 70°C .

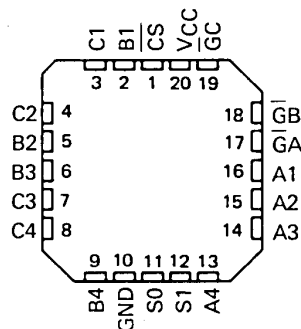
FUNCTION TABLE

INPUTS						TRANSFERS BETWEEN BUSES		
$\overline{\text{CS}}$	S1	S0	$\overline{\text{GA}}$	$\overline{\text{GB}}$	$\overline{\text{GC}}$	'LS440	'LS441	'LS444
						'LS442	'LS443	'LS448
H	X	X	X	X	X	None	None	None
X	H	H	X	X	X	None	None	None
X	X	X	H	H	H	None	None	None
X	L	L	X	H	H	None	None	None
X	L	H	H	X	H	None	None	None
X	H	L	H	H	X	None	None	None
L	L	L	X	L	L	$A \rightarrow B, A \rightarrow C$	$A \rightarrow B, \overline{A} \rightarrow C$	$A \rightarrow B, A \rightarrow C$
L	L	H	L	X	L	$B \rightarrow C, B \rightarrow A$	$\overline{B} \rightarrow C, \overline{B} \rightarrow A$	$B \rightarrow C, \overline{B} \rightarrow A$
L	H	L	L	L	X	$C \rightarrow A, C \rightarrow B$	$\overline{C} \rightarrow A, \overline{C} \rightarrow B$	$\overline{C} \rightarrow A, C \rightarrow B$
L	L	L	X	L	H	$A \rightarrow B$	$\overline{A} \rightarrow B$	$\overline{A} \rightarrow B$
L	L	H	H	X	L	$B \rightarrow C$	$\overline{B} \rightarrow C$	$B \rightarrow C$
L	H	L	L	H	X	$C \rightarrow A$	$\overline{C} \rightarrow A$	$\overline{C} \rightarrow A$
L	L	L	X	H	L	$A \rightarrow C$	$\overline{A} \rightarrow C$	$\overline{A} \rightarrow C$
L	L	H	L	X	H	$B \rightarrow A$	$\overline{B} \rightarrow A$	$\overline{B} \rightarrow A$
L	H	L	H	L	X	$C \rightarrow B$	$\overline{C} \rightarrow B$	$C \rightarrow B$

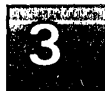
SN54LS' ... J PACKAGE
SN74LS' ... DW, J OR N PACKAGE
(TOP VIEW)



SN54LS' ... FK PACKAGE
SN74LS' ... FN PACKAGE
(TOP VIEW)



DEVICE	OUTPUT	LOGIC
'LS440	Open-Collector	True
'LS441	Open-Collector	Inverting
'LS442	3-State	True
'LS443	3-State	Inverting
'LS444	3-State	True/Inverting
'LS448	Open-Collector	True/Inverting



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PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

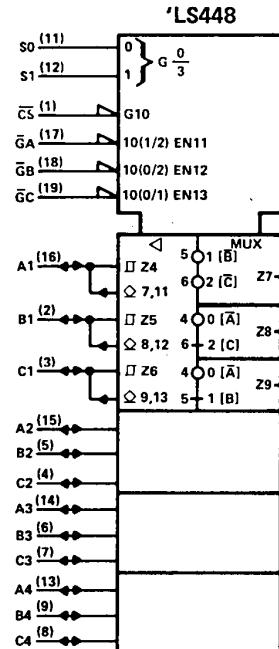
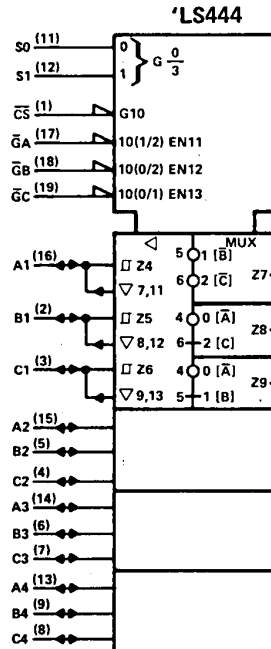
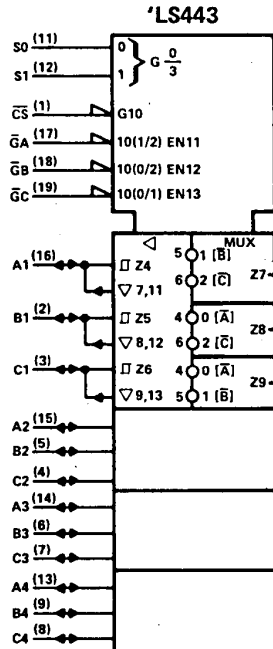
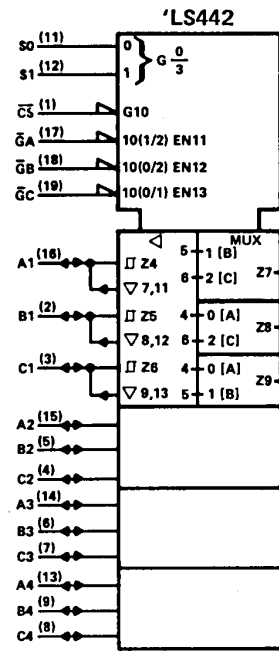
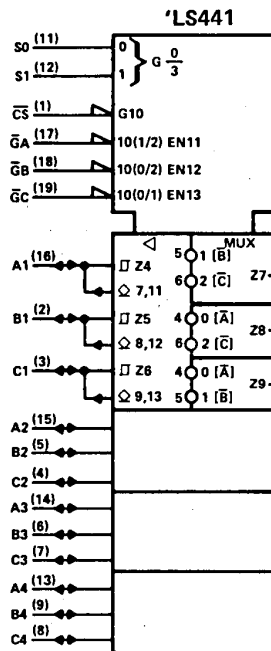
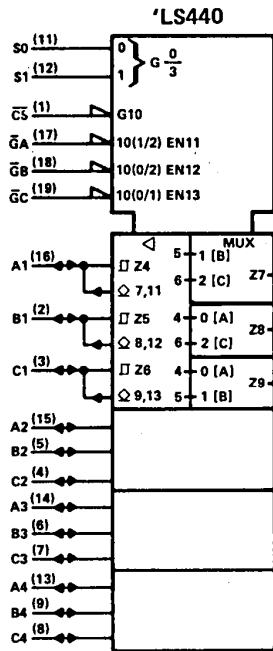
TEXAS
INSTRUMENTS

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TYPES SN54LS440 THRU SN54LS444, SN54LS448,
 SN74LS440 THRU SN74LS444, SN74LS448
 QUADRUPLE TRIDIRECTIONAL BUS TRANSCEIVERS

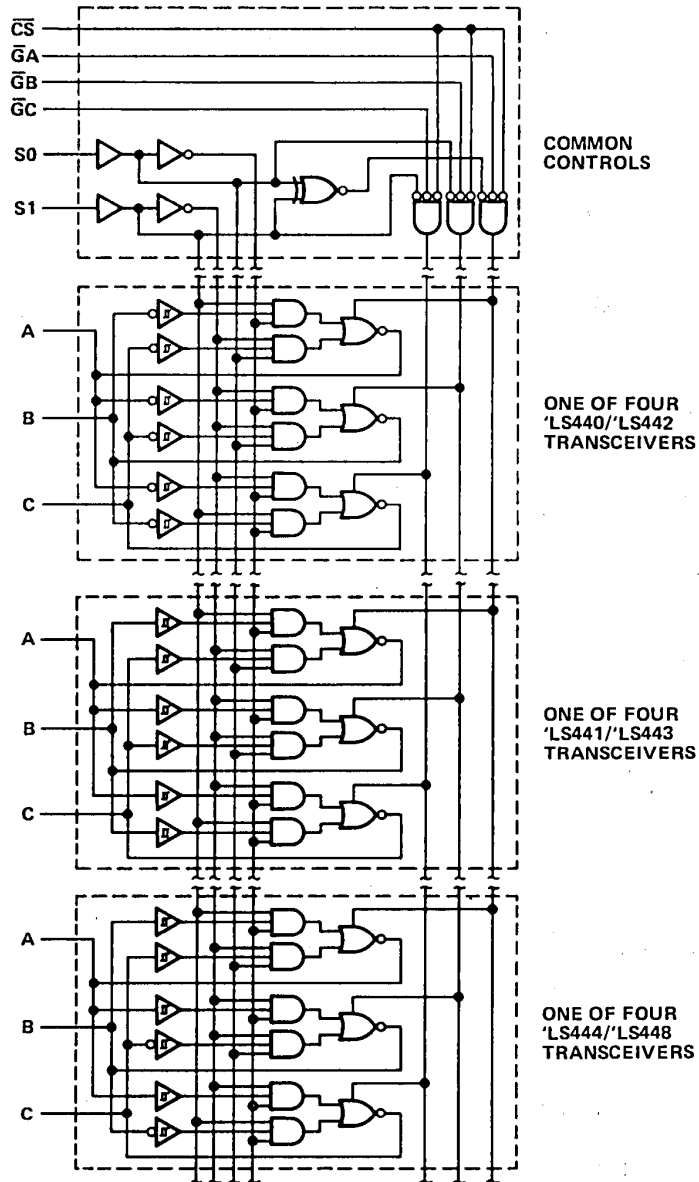
logic symbols



Pin numbers shown on logic notation are for DW, J or N packages.

TYPES SN54LS440 THRU SN54LS444, SN54LS448,
SN74LS440 THRU SN74LS444, SN74LS448
QUADRUPLE TRIDIRECTIONAL BUS TRANSCEIVERS

logic diagram (composite showing one of four transceivers from each type, positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS'	-55°C to 125°C
SN74LS'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

**TYPES SN54LS440, SN54LS441, SN54LS448,
SN74LS440, SN74LS441, SN74LS448
QUAD TRIDIRECTIONAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS**

recommended operating conditions

	SN54LS440 SN54LS441 SN54LS448			SN74LS440 SN74LS441 SN74LS448			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}	5.5			5.5			V
Low-level output current, I_{OL}	12			24			mA
Operating free-air temperature, T_A	-55			125			C

NOTE 1: Voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS*			SN74LS*			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage		0.5			0.6			V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	-1.5			-1.5			V
Hysteresis ($V_{T+} - V_{T-}$) A,B,C input	$V_{CC} = \text{MIN}$	0.1	0.4		0.2	0.4	V	
I_{OH} High-level output current	$V_{CC} = \text{MIN}, V_{OH} = 5.5 \text{ V}, V_{IL} = V_{IL\text{max}}$	100			100			μA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL\text{max}}$	$I_{OL} = 12 \text{ mA}$		0.25	0.4	0.25	0.4	V
		$I_{OL} = 24 \text{ mA}$				0.35	0.5	V
I_I Input current at maximum input voltage	A,B,C input	$V_{CC} = \text{MAX}$		$V_I = 5.5 \text{ V}$		0.1		mA
	All others	$V_{CC} = \text{MAX}$		$V_I = 7 \text{ V}$		0.1		
I_{IH} High-level input current		$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20		20		μA
I_{IL} Low-level input current		$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.4		-0.4		mA
I_{CC} Supply current	Outputs low	$V_{CC} = \text{MAX}, \text{Outputs open}$		62	90	62	90	mA
	Outputs disabled			64	95	64	95	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

switching characteristics at $V_{CC} = 5 \text{ V}, R_L = 667 \Omega, C_L = 45 \text{ pF}, T_A = 25^\circ\text{C}$, see note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'LS440			'LS441			'LS448			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high level output	A	B	24	35		21	30		21	30	ns	
	A	C	24	35		21	30		21	30		
	B	A	24	35		21	30		21	30		
	B	C	24	35		21	30		24	35		
	C	A	24	35		21	30		21	30		
	C	B	24	35		21	30		24	35		
t_{PHL} Propagation delay time, high-to-low level output	A	B	20	30		9	15		9	15	ns	
	A	C	20	30		9	15		9	15		
	B	A	20	30		9	15		9	15		
	B	C	20	30		9	15		20	30		
	C	A	20	30		9	15		9	15		
	C	B	20	30		9	15		20	30		
t_{PLH} Propagation delay time, low-to-high level output	any \bar{G}	A, B, C	29	45		23	35		25	40	ns	
	S0, S1	A, B, C	33	50		27	40		26	40		
	\bar{CS}	A, B, C	31	45		26	40		25	40		
t_{PHL} Propagation delay time, high-to-low level output	any \bar{G}	A, B, C	27	40		20	30		22	35	ns	
	S0, S1	A, B, C	32	50		26	40		27	40		
	\bar{CS}	A, B, C	28	45		21	30		22	35		

NOTE 2: See General Information Section for load circuits and voltage waveforms.

**TYPES SN54LS442, SN54LS443, SN54LS444,
SN74LS442, SN74LS443, SN74LS444**
QUAD TRIDIRECTIONAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

	SN54LS442 SN54LS443 SN54LS444			SN74LS442 SN74LS443 SN74LS444			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-12			-15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS*			SN74LS*			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.5			0.6	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
Hysteresis ($V_{T+} - V_{T-}$) A,B,C input	$V_{CC} = \text{MIN}$	0.1	0.4		0.2	0.4		V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL\text{max}}$	$I_{OH} = -3 \text{ mA}$	2.4	3.4	2.4	3.4		V
		$I_{OH} = \text{MAX}$	2		2			
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL\text{max}}$	$I_{OL} = 12 \text{ mA}$	0.25	0.4	0.25	0.4		V
		$I_{OL} = 24 \text{ mA}$			0.35	0.5		
I_{OZH} Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}, \overline{CS}$ at 2 V	$V_O = 2.7 \text{ V}$		20		20	μA	
I_{OZL} Off-state output current, low-level voltage applied		$V_O = 0.4 \text{ V}$		-400		-400		
I_I Input current at maximum input voltage	A, B, C	$V_{CC} = \text{MAX}$	$V_I = 5.5 \text{ V}$		0.1		0.1	mA
	Others		$V_I = 7 \text{ V}$		0.1		0.1	
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20		20	μA	
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4		-0.4	mA	
I_{OS} Short circuit output current	$V_{CC} = \text{MAX}$			-40		-225	mA	
I_{CC} Supply current	Outputs low	$V_{CC} = \text{MAX},$ Outputs open		62	90	62	90	mA
	Outputs at Hi-Z			64	95	64	95	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

¶ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

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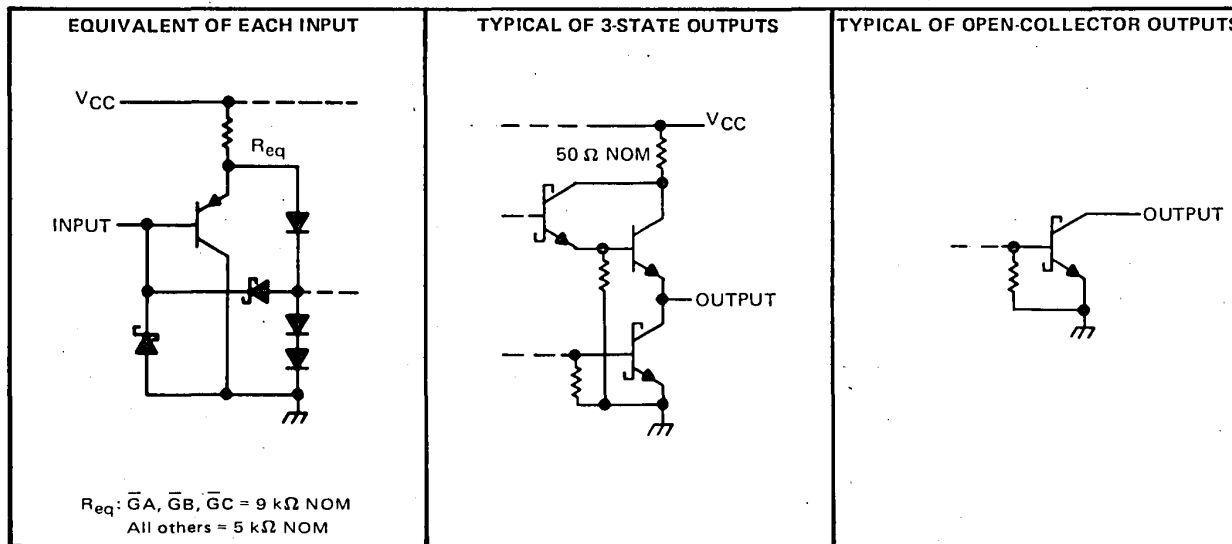
**TYPES SN54LS442, SN54LS443, SN54LS444,
SN74LS442 THRU SN74LS443, SN74LS444
QUAD TRIDIRECTIONAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS**

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, see note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS442			'LS443			'LS444			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH} Propagation delay time, low-to-high level output	A	B	C _L = 45 pF, R _L = 667 Ω		10	14		9	14		9	14	ns
	A	C		10	14	9	14	9	14				
	B	A		10	14	9	14	9	14				
	B	C		10	14	9	14	10	14				
	C	A		10	14	9	14	9	14				
	C	B		10	14	9	14	10	14				
t _{PHL} Propagation delay time, high-to-low level output	A	B		13	20	7	13	7	13	ns			
	A	C		13	20	7	13	7	13				
	B	A		13	20	7	13	7	13				
	B	C		13	20	7	13	13	20				
	C	A		13	20	7	13	7	13				
	C	B		13	20	7	13	13	20				
t _{PZL} Output enable time to low level	Any \bar{G}	A, B, C		22	33	22	33	22	33	ns			
	S0 or S1	A, B, C		28	42	28	42	28	42				
	\bar{CS}	A, B, C		23	36	24	36	23	36				
t _{PZH} Output enable time to high level	\bar{G}, S \bar{CS}	A, B, C		21	32	20	32	24	32	ns			
t _{PLZ} Output disable time from low level	\bar{G}, S \bar{CS}	A, B, C		14	25	15	25	14	25	ns			
t _{PHZ} Output disable time from high level	\bar{G}, S \bar{CS}	A, B, C		14	25	15	25	14	25	ns			

NOTE 2: See General Information Section for load circuits and voltage waveforms.

schematics of inputs and outputs



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