

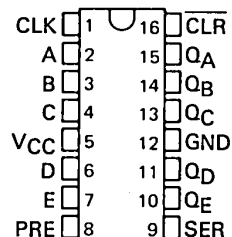
TYPES SN5496, SN54L96, SN54LS96, SN7496, SN74LS96 5-BIT SHIFT REGISTERS

MARCH 1974—REVISED DECEMBER 1983

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

SN5496, SN54LS96 ... J OR W PACKAGE
SN54L96 ... J PACKAGE
SN7496 ... J OR N PACKAGE
SN74LS96 ... D, J OR N PACKAGE
(TOP VIEW)

TYPE	TYPICAL	
	PROPAGATION DELAY TIME	POWER DISSIPATION
'96	25 ns	240 mW
'L96	50 ns	120 mW
'LS96	25 ns	60 mW



description

These shift registers consist of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs for all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to a low output level by applying a low-level voltage to the clear input while the preset is inactive (low). Clearing is independent of the level of the clock input.

The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to the individual preset inputs (A, B, C, D, and E) and a high-level load pulse is applied to the preset enable input. Presetting like clearing is independent of the level of the clock input.

Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be set up at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be high and the preset or preset enable inputs must be low when clocking occurs.

For chip carrier information on SN54LS96 and SN74LS96, contact the factory.

FUNCTION TABLE

CLEAR	PRESET ENABLE	PRESET					CLOCK	SERIAL	OUTPUTS				
		A	B	C	D	E			QA	QB	QC	QD	QE
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	L	X	QA0	QB0	QC0	QD0	QE0
H	H	H	L	H	L	H	L	X	H	QB0	H	QD0	H
H	L	X	X	X	X	X	L	X	QA0	QB0	QC0	QD0	QE0
H	L	X	X	X	X	X	↑	H	H	QAn	QBn	Qcn	QDn
H	L	X	X	X	X	X	↑	L	L	QAn	QBn	Qcn	QDn

H = high level (steady state), L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

QA0, QB0, etc = the level of QA, QB, etc, respectively before the indicated steady-state input conditions were established.

QAn, QBn, etc = the level of QA, QB, etc, respectively before the most-recent ↑ transition of the clock.

PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

3-385

3
TTL DEVICES

TYPES SN5496, SN7496

5-BIT REGISTERS

recommended operating conditions

	SN5496			SN7496			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		10	0		10	MHz
Width of clock input pulse, $t_w(\text{clock})$	35			35			ns
Width of preset and clear input pulse, t_w	30			30			ns
Serial input setup time, t_{SU} (see Figure 1)	30			30			ns
Serial input hold time, t_h (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN5496			SN7496			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -400 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	High-level input current	any input except preset enable			40			40	μ A
		preset enable			200			200	
I_{IL}	Low-level input current	any input except preset enable			-1.6			-1.6	mA
		preset enable			-8			-8	
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-20		-57	-18		-57	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, See Note 3		48	68		48	79	mA

† For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{PLH} Propagation delay time, low-to-high-level output from clock	$C_L = 15 \text{ pF}, R_L = 400 \Omega,$ See Figure 1		25	40	ns	
t_{PHL} Propagation delay time, high-to-low-level output from clock			25	40	ns	
t_{PLH} Propagation delay time, low-to-high-level output from preset or preset enable				28	35	ns
t_{PHL} Propagation delay time, high-to-low-level output from clear					55	ns

TYPE SN54L96 5-BIT SHIFT REGISTER

recommended operating conditions

		SN54L96			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			-0.2	mA
I_{OL}	Low-level output current			8	mA
f_{clock}	Clock frequency	0		5	MHz
t_w	Width of clock, preset, or clear input	100			ns
t_{su}	Serial input setup time (See Figure 1)	100			ns
t_h	Serial input hold time (See Figure 1)	0			ns
T_A	Operating free-air temperature	-55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54L96			UNIT
		MIN	TYP‡	MAX	
V_{OH}	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -0.2 \text{ mA}$	2.4	3.2		V
V_{OL}	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 8 \text{ mA}$		0.2	0.4	V
I_I	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH}	Any input except preset enable	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$		20	μA
	Preset enable			0.1	mA
I_{IL}	Any input except preset enable	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$		-0.8	mA
	Preset enable			-4	mA
I_{OSS}	$V_{CC} = \text{MAX}$	-10		-29	mA
I_{CC}	$V_{CC} = \text{MAX}$, See Note 3		24	34	mA

† For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Clock	Any	$R_L = 800 \Omega$, See Figure 1	$C_L = 15 \text{ pF}$	50	80	ns
t_{PHL}					50	80	ns
t_{PLH}	Preset or Preset enable				56	70	ns
t_{PHL}	Clear					110	ns



TTL DEVICES

TEXAS INSTRUMENTS

POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

3-389

TYPES SN54LS96, SN74LS96

5-BIT SHIFT REGISTERS

recommended operating conditions

	SN54LS96			SN74LS96			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock input pulse, $t_w(\text{clock})$	20			20			ns
Width of preset and clear input pulse, t_w	30			30			ns
Serial input setup time, t_{setup} (see Figure 1)	30			30			ns
Serial input hold time, t_{hold} (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS96		SN74LS96		UNIT		
			MIN	TYP‡	MAX	MIN		TYP‡	MAX
V_{IH}	High-level input voltage		2			2	V		
V_{IL}	Low-level input voltage				0.7		0.8	V	
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5		-1.5	V	
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5	V	
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$			0.25	0.4	0.25	0.4	V
I_I	Input current at maximum input voltage	Preset enable			0.5		0.5	mA	
		All others			0.1		0.1		
I_{IH}	High-level input current	Preset enable			100		100	μ A	
		All others			20		20		
I_{IL}	Low-level input current	Preset enable			-2		-2	mA	
		All others			-0.4		-0.4		
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-20		-100		-20	-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}, \text{ See Note 3}$		12	20		12	20	mA

† For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 3: I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{PLH} Propagation delay time, low-to-high-level output from clock	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega, \text{ See Figure 1}$		25	40	ns	
t_{PHL} Propagation delay time, high-to-low-level output from clock			25	40	ns	
t_{PLH} Propagation delay time, low-to-high-level output from preset or preset enable				28	35	ns
t_{PHL} Propagation delay time, high-to-low-level output from clear					55	ns

3

TTL DEVICES

