

TYPES SN54LS396, SN74LS396 OCTAL STORAGE REGISTERS

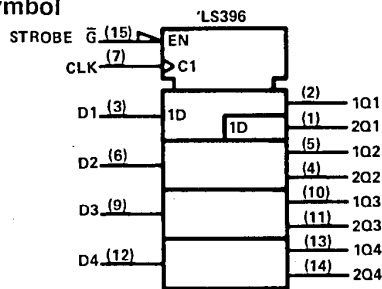
D2329, MARCH 1977—PREVISED DECEMBER 1983

- Parallel Access
- Typical Propagation Delay Time . . . 20 ns
- Typical Power Dissipation . . . 120 mW
- Applications:
N-Bit Storage Files
Hex/BCD Serial-To-Parallel Converters

description

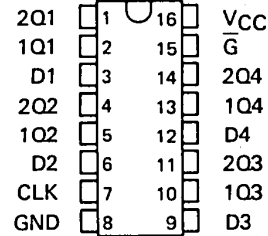
These octal registers are organized as two 4-bit bytes of storage. Upon application of a positive-going clock signal, the information stored in byte 1 is transferred into byte 2 as a new 4-bit byte is loaded into the byte 1 location via the four data lines. The full 8-bit word is available at the outputs after two clock cycles. Both the clock and the strobe lines are fully buffered.

logic symbol

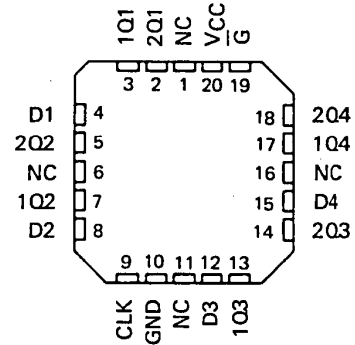


Pin numbers shown on logic notation are for D, J or N packages.

SN54LS396 . . . J OR W PACKAGE
SN74LS396 . . . D, J OR N PACKAGE
(TOP VIEW)



SN54LS396 . . . FK PACKAGE
SN74LS396 . . . FN PACKAGE
(TOP VIEW)



NC - No internal connection

FUNCTION TABLE

| INPUTS | | OUTPUTS | | | | | | | | | | | |
|-----------------|-------|---------|----|----|----|--------|-----|-----|-----|------------------|------------------|------------------|------------------|
| STROBE G-bar | CLOCK | DATA | | | | BYTE 1 | | | | BYTE 2 | | | |
| | | D1 | D2 | D3 | D4 | 1Q1 | 1Q2 | 1Q3 | 1Q4 | 2Q1 | 2Q2 | 2Q3 | 2Q4 |
| H | X | X | X | X | X | L | L | L | L | L | L | L | L |
| L | ↑ | a | b | c | d | a | b | c | d | 1Q1 _n | 1Q2 _n | 1Q3 _n | 1Q4 _n |

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)

↑ = transition from low to high level

1Q1_n, 1Q2_n, 1Q3_n, 1Q4_n = the level of 1Q1, 1Q2, 1Q3, and 1Q4, respectively, before the most recent ↑ transition of the clock.

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

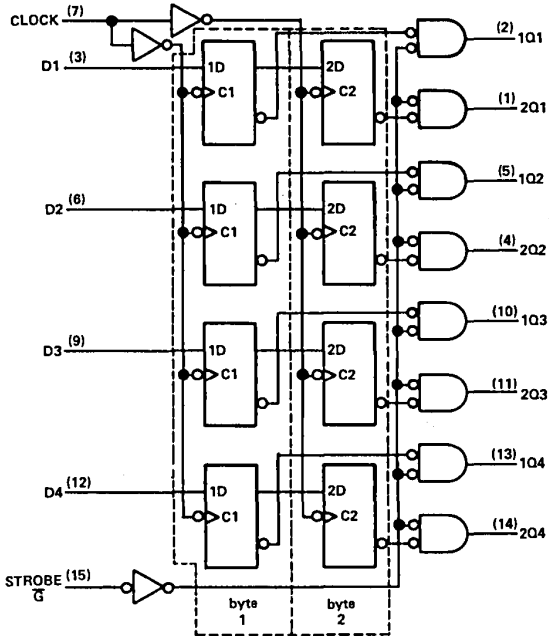
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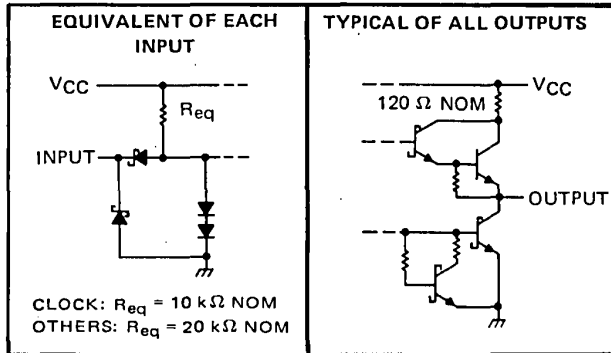
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TYPES SN54LS396, SN74LS396 OCTAL STORAGE REGISTERS

logic diagram



schematics of inputs and outputs



Pin numbers shown on logic notation are for D, J or N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage | 7 V |
| Operating free-air temperature range: SN54LS396 | -55°C to 125°C |
| SN74LS396 | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

| | SN54LS396 | | | SN74LS396 | | | UNIT |
|---------------------------------------|-----------|-----|------|-----------|-----|------|---------------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, V_{CC} | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, I_{OH} | | | -400 | | | -400 | μA |
| Low-level output current, I_{OL} | | | 4 | | | 8 | mA |
| Clock frequency, f_{clock} | 0 | | 30 | 0 | | 30 | MHz |
| Width of clock pulse, t_w | 20 | | | 20 | | | ns |
| Setup time, t_{su} | 20 | | | 20 | | | ns |
| Hold time, t_h | 5 | | | 5 | | | ns |
| Operating free-air temperature, T_A | -55 | | 125 | 0 | | 70 | °C |

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | SN54LS396 | | | SN74LS396 | | | UNIT | |
|-----------------|--|---|------------------------|------|------|-----------|------|-----|------|----|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | | |
| V _{IH} | High-level input voltage | | 2 | | | 2 | | | V | |
| V _{IL} | Low-level input voltage | | 0.7 | | | 0.8 | | | V | |
| V _{IK} | Input clamp voltage | V _{CC} = MIN, I _I = -18 mA | -1.5 | | | -1.5 | | | V | |
| V _{OH} | High-level output voltage | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -400 μA | 2.5 | 3.4 | | 2.7 | 3.4 | | V | |
| V _{OL} | Low-level output voltage | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX | I _{OL} = 4 mA | | 0.25 | 0.4 | 0.25 | | 0.4 | V |
| | | | I _{OL} = 8 mA | | | | 0.35 | | 0.5 | |
| I _I | Input current at maximum input voltage | V _{CC} = MAX, V _I = 7 V | Clock input | | 0.2 | | 0.2 | | mA | |
| | | | Other inputs | | 0.1 | | 0.1 | | | |
| I _{IH} | High-level input current | V _{CC} = MAX, V _I = 2.7 V | Clock input | | 40 | | 40 | | μA | |
| | | | Other inputs | | 20 | | 20 | | | |
| I _{IL} | Low-level input current | V _{CC} = MAX, V _I = 0.4 V | Clock input | | -0.8 | | -0.8 | | mA | |
| | | | Other inputs | | -0.4 | | -0.4 | | | |
| I _{OS} | Short-circuit output current§ | V _{CC} = MAX | -20 | -100 | -20 | -100 | | | mA | |
| I _{CC} | Supply current | V _{CC} = MAX, See Note 2 | 24 | | 40 | | 24 | | 40 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--|---|-----|-----|-----|------|
| t _{PLH} | Propagation delay time, low-to-high-level output from clock | C _L = 15 pF, R _L = 2 kΩ, See Note 3 | 20 | | 30 | ns |
| t _{PHL} | Propagation delay time, high-to-low-level output from clock | | 20 | | 30 | |
| t _{PLH} | Propagation delay time, low-to-high-level output from strobe | | 20 | | 30 | ns |
| t _{PHL} | Propagation delay time, high-to-low-level output from strobe | | 20 | | 30 | |

NOTE 3: See General Information Section for load circuits and voltage waveforms.



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